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30 GHz MONOLITHIC RECEIVE MODULE

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16. Abstract

This report covers the technical achievements and deliveries made during the entire duration of the program to develop a 30 GHz monolithic receive module for communication feed array applications, to deliver submodules and 30 GHz monolithic receive modules for experimental evaluation. Key requirements include an overall receive module noise figure of 5 dB, a 30 dB RF-to-IF gain with six levels of intermediate gain control, a 5 bit phase shifter, and a maximum power consumption of 250 mW. In addition, the monolithic receive module design addresses a cost goal of less than $1,000 (1980 dollars) per receive module in unit buys of 5,000 or more, and a mechanical configuration that is applicable to a space-borne phase array system. An additional task for the development and delivery of 32 GHz phase shifter IC for NASA/JPL deep space communication is also described.

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TABLE CAPTIONS

FIGURE CAPTIONS

1. SUMMARY

This report covers the progress made during the entire period of a program (Nov. 1982 to Nov. 1990) to develop a 30 GHz monolithic receive module for communication antenna feed array applications, to deliver submodules and 30 GHz monolithic modules for experimental evaluation and to develop and deliver functional four bit phase shifters (as an add-on contract) to NASA/LeRC and JPL. Key requirements for receive module include an overall receive module noise figure of 5 dB, a 30 dB RF-to-IF gain with six levels of intermediate gain control, a 5 bit phase shifter, and a maximum power consumption of 250 mW. Key requirement for the add-on four bit phase shifter is minimum loss (approximately 8 dB) over the bandwidth 31-33 GHz. In addition, the monolithic receive module design addresses a cost goal of less than $1,000 (1980 dollars) per receive module in unit buys of 5,000 or more, and a mechanical configuration that is applicable to a space-borne phased array system. These requirements are summarized as performance goals in Table 1-1.

In Table 1-2 a summary of technical accomplishments is listed out during the whole program period. The accomplishments are shown with the task numbers. Except the task VII, which was discontinued for lack of funds, all other tasks were completed along with the delivery requirements.

In Figure 1-1 and 1-2 we show the submodule functions of receive module and block diagram of overall monolithic receiver with gain budgets. The monolithic receiver contains four function RF chips namely LNA, lPS, GC, and RF/IF mixer. The main design objective is to interconnect the submodules to produce the complete receive module.

In Section 2 we will discuss each technical effort by task number. The circuit layout, experimental results, and conclusions will be given for all submodules. In section 3 we will discuss future improvement plans and recommendations for integration of the module.

TABLE 1-1. NASA'S KEY PERFORMANCE GOALS

Design Parameter	Performance Goal
A. RECEIVE MODULE	
RF Band	27.5 - 30 GHz
IF Center Frequency	Between 4 -8 GHz
Noise Figure at Room Temperature	$\leq$ 5 dB
RF/IF Gain	< 30 dB at highest level of gain control
Gain Control	At least six levels: 30, 27, 24, 20, 17 dB and Off
Phase Control	5 bits, each bit $\pm$ 3° at band center
Module Power Consumption	250 mW in all states. In OFF state, 25 mW
Phase and Gain Control	Operate on digital input
Mechanical Design	Fully monolithic construction, compatible with 30 GHz spaceborne phase array applications
Unit Cost	Less than $1000 (1980 dollars) in unit buys of 5000 or more
B. PHASE SHIFTER (add-on)	
RF Band	31-33 GHz
No. of Bits	4 (180°, 90°, 45°, 22.5°)
Insertion Loss	$\leq$ 8 dB

TABLE 1-2. SUMMARY OF TECHNICAL ACCOMPLISHMENTS WITH TASK NUMBERS

TASK #	DESCRIPTION	COMMENTS
I	Device and circuit design for receive module	Completed in the first[1] year.
II	Design, fabrication, and evaluation of 5-bit phase shifter for receive module using self-aligned gate (SAG) process	Initial fabrication and evaluation completed in the first[1] year. Delivery of 25 phase shifters (out of 100 required) completed in the second[2] year. Delivery of the remaining 80 phase shifters completed in the third[3] year.
III	Design, fabrication, and evaluation of the gain control block for receive module, using dual gate FET amplifiers.	Initial design and layout completed in the first[1] year. First run and initial evaluation of a hybrid amplifier completed in the second[2] year. A redesign of the gain control block was completed in the third[3] year. Demonstration of a two-stage monolithic GCA (with 13 dB gain control) and delivery of 100 GCA chips completed in the fifth[5] year.
IV	Design and development of ion-implanted mixer (RF/IF submodule) for receive module.	Development of critical mixer component (Schottky diode compatible with FET technology) initiated and preliminary results obtained in the third[3] year. Design, fabrication, and evaluation of RF/IF mixer, LO 22 GHz amplifier, IF amplifier completed in the fourth[4] and fifth[5] years. Delivery of 49 dc screened RF/IF mixer IC's and one mounted mixer chip completed in the sixth[6] year and 10 LO amplifier chips completed in the fifth[5] year.

TABLE 1-1. SUMMARY OF TECHNICAL ACCOMPLISHMENTS WITH TASK NUMBERS (cont.)

TASK #	DESCRIPTION	COMMENTS
V	Design, fabrication, and evaluation of ion implanted LNA for receive module	FET design for LNA completed in the first[1] year. Device evaluation completed in the second[2] year. Two stage LNA MMIC (7 dB gain and 6.2 dB NF) demonstrated and 10 LNA chips delivered at the end of fifth[5] year.
VI	Interconnection of individual submodules (LNA, phase shifter, GCA, and RF/IF mixer) into a receive module with bond wires.	Overall drawing and dimension for the interconnected receive module completed in the fourth[4] year. Development, demonstration and delivery of interconnected submodules as receive module (3 in total) completed in the fifth[5] year.
VII	Development of monolithically integrated receive module with three RF functions namely LNA, phase shifter and GCA, and digital control circuits for the phase shifter.	First fabrication of a monolithic CTS receiver initiated in the fifth[5] year with three chips integrated on chip, namely a two-stage LNA, a reduced size phase shifter and digital control logic in the fifth[5] year. RF evaluation of the two-stage LNA circuit produced unsatisfactory results in the sixth[6] year; a few process problems detected, but no second iteration planned due to lack of funding; the effort stopped in the sixth[6] year.
VIII	Assessment of Honeywell technology and the results during the program, and comparison with the available technologies responded in the technical literature.	A report submitted for the receive module in April, 1988.
IX	Record keeping of device and circuit developed.	Maintained from the beginning of the program.

TABLE 1-2. SUMMARY OF TECHNICAL ACCOMPLISHMENTS WITH TASK NUMBERS (cont.)

X	Reporting.	Updated monthly and annual technical progress reports, monthly and quarterly financial and management reports submitted as required by the contract.
XI	Design, fabrication, evaluation, and delivery of four bit phase shifter (31-33 GHz) for NASA/LeRC and JPL.	First design iteration and evaluation completed in the seventh[7] year of the program. Second iteration, evaluation, and RF tested phase shifter chips delivered to NASA/LeRC (50 chips) and JPL (35 chips) at end of the eighth[8] year.

1. First year - November 1982-October 1983
2. Second year - November 1983-October 1984
3. Third year - November 1984-October 1985
4. Fourth year - November 1985-October 1986
5. Fifth year - November 1986-October 1987
6. Sixth year - November 1987-October 1988
7. Seventh year - November 1988-October 1989
8. Eighth year - November 1989-October 1990

2. PROGRAM IMPLEMENTATION BY TASKS

The objective of this program was to develop a 30 GHz monolithic receive module for communication antenna feed array applications, to deliver submodules and 30 GHz receive modules for experimental evaluation. During the course of this program, an extra task was added to develop and deliver 32 GHz 4-bit phase shifters for NASA/JPL applications. Key performance and design goals are mentioned in Table 1-1. In Table 1-2 we summarized the tasks and their status. In the following selections, we will discuss different tasks and the progress made over the course of this program. We will go over the tasks serially.

2.1 Task I - Receive Module Design

This task was completed in the first year of the program (Nov. 1982-Nov. 1983). The effort was directed towards a detailed initial design of the complete receive module and four submodules. The four submodules include low noise amplifier (LNA), a phase shifter (PS), a gain control (GC) and an RF/IF mixer (RF/IF). The work was also done on the device design that would be suitable for specific submodule. Ion implantation was chosen as the baseline technology, to make the receive module cost effective (the cost goal was to have the monolithic module under $1,000).

2.1.1 Phase Shifter Design

A more comprehensive design was completed for the phase shifter submodule during this task than the other three submodules. The reason was, the phase shifter delivery was due early in the program. Two types of phase shifter topology were examined initially [1]; one with shunt FET switches and the second one with series FET switches. The latter approach was ultimately chosen because of ease of microstrip circuit layout and less GaAs area. The final topology for the phase shifter had three switched line bits (180°, 90°, and 45°), each using four series FET switches and one loaded line bit (22.5°) using two shunt FET switches. A detailed loss analysis and topology selection procedure for the phase shifter is given in section 1.1.2 of the report [1]. Figure 2-1 shows the chip layout and the schematic of 180° bit. The design includes 400 μm wide FETs with loops for given off state resonance at the center of the band. The electrical line length difference between two states gives the required phase shift. To maintain the same and low insertion loss between the two states, the "ON" state insertion loss of the switches should be as low as possible and the "OFF" state insertion (or isolation) as high as one could achieve. By choosing a proper gate width, it is possible to come to a compromise between the isolation and insertion loss. The methodology is discussed in [1], section 1.1.2. Figure 2.2 shows the calculated performance of a 3-bit switched line phase shifter, (180°, 90°, and 45°) and Figure 2-3 shows the calculated

insertion loss envelope for such a 3-bit phase shifter. A four bit version with 22.5° bit as the loaded line was fabricated later in Task II.

2.1.2 Gain Control

There were two critical requirements for this submodule - a maximum NF of 14 dB at 1 dB attenuation state and a maximum allowable phase change of ±5° over 13 dB change in gain. The submodule was to provide five levels of RF to IF gain (30, 27, 24, 20, and 17 dB) and an OFF state. Keeping the above two requirements in mind, a two-stage dual-gate FET amplifier, followed by a variable passive attenuator was chosen for the gain control. Figure 2-4 shows such a scheme. Initial design on a two-stage dual-gate FET amplifier was made under the Task I using 100 μm FET. Figure 2-5 shows the circuit schematic and computer optimized gain of such a two-stage amplifier. Subsequent iteration of the gain control would include the passive attenuator on the same chip.

2.1.3 RF/IF Submodule

This submodule was to provide three functions:

1. Convert the 27.5 to 30 GHz input RF signal to the IF (5.5 GHz) in a mixer;
2. Amplify an external reference signal to provide a local oscillator input (22 GHz) to the mixer;
3. Amplify and buffer the mixer IF output to drive the IF amplifiers.

Balanced Schottky Diode Mixer - The baseline mixer design approach was the balanced Schottky diode mixer with a rat race hybrid shown integrated with the other elements of the RF/IF submodule in Figure 2-6. The input signal inserted on the right side of the chip, is shifted in phase by 90° to one mixer diode, and 270° to the other. The diodes are connected 180° out of phase to suppress noise from the local oscillator amplifier and reference signal, while combining the IF signals in phase. The diodes are connected to IF frequency and dc ground by vias through the substrate; open circuited stubs are used to ensure a high quality ground for the signal and local oscillator.

The mixer employs a pair of surface oriented Schottky barrier diodes so that fabrication is compatible with that of the FETs. Good results [10] were reported using many small diodes in

parallel to lower the overall series resistance. The diodes that were used in this program is shown in Figure 2-7. By decreasing the capacitance of the individual diodes while maintaining an approximately constant value of series resistance these methods should be useful at 30 GHz.

22 GHz LO Amplifier - The requirements for the 22 GHz local oscillator included a gain of 24 dB and a noise figure of 5 dB. Other than frequency, the requirements are similar to the RF low noise amplifier used for the "front end" of the receiver. FETs with 100 μm gate width were used for the LO amplifier.

To assess the noise figure and gain trade-offs for the 100 micron FET at 22 GHz, the noise figure and gain circles were calculated and plotted on the Smith Chart as shown in Figure 2-8. The 3 stage amplifier shown in Figure 2-9 was designed to achieve the required 24 dB total gain and yet realize the source impedance (e.g., $z_s = .6 + j\ 1.2$) as seen by the first stage especially, to be in the region of minimum noise using Figure 2-8 as a guideline.

IF Amplifier - The IF amplifier was primarily needed to buffer the mixer output to drive lower impedance transmission lines. The requirements included 5 dB gain from 5.5 to 8 GHz. A preliminary design using a 150 micron FET equivalent circuit in a single stage common source configuration was developed. The circuit design made use of the so-called "lossy" match technique, i.e., frequency dependent resistive loss was used to obtain flat gain over a 60% fractional bandwidth. A gain of about 6 dB was achieved from 5 to 9 GHz.

2.1.4 30 GHz Low Noise Amplifier Submodule

Five stages of GaAs FET amplification were to be used in the LNA. The first three stages were designed for a noise figure of 4 dB and an associated gain of 6 dB, while the last two stages were budgeted for slightly higher gains and noise. The number of LNA stages was chosen large enough to achieve sufficient front end gain to minimize the effects of noise figure contributions and losses of following submodule components on the total noise figure of the receive module, which was to be 5 dB.

Because of the low dc power consumption budget (3V and 20 mA for the complete LNA) and the theoretically predicted improvement of device noise figure with smaller gate widths, the FETs used in the LNA had gate widths of 100 microns with 0.25 μm length. Although even small gate widths are desirable from an efficiency and noise figure point of view, a lower limit on gate width exists because of impedance matching considerations. In particular, too small a gate width results in high impedance levels which are difficult to match to 50 ohms (especially for the FET output

circuit). This is due to design constraints imposed by the physical limitations of monolithically fabricated reactive circuit elements. The most direct consequence of this difficulty is bandwidth reduction due to large impedance transformation ratios.

An initial design for the five stage amplifier is shown in Figure 2-10. The FET equivalent circuit discussed in Section 2.1.5 was used for the FET devices. As shown in the figure the gain is the required 32 dB $\pm$ .5 dB from 27 to 31 GHz. Input impedance matching took into account the gain/noise figure trade-off especially for the first stage. As shown in the figure the design utilized similar circuit elements which were relatively easy to realize monolithically on a 0.15 mm thick substrate.

2.1.5 Device Design

Under Task I, device design was directed towards 400 micron switching FETs for phase shifter design and 100 μm FET for LNA design. For the switching FETs, the main design requirement was low "ON" resistance; SAG (self-aligned gate) technology was found suitable to meet this requirement. It was estimated a source drain resistance of 5 Ω (for 400 μm) could be achieved with this technology to bring the insertion loss to 1.5-2 dB per bit.

The devices for low noise amplifier had to meet the following requirements:

(i) low noise figure with sufficient associated gain
(ii) low power consumption
(iii) processing reproducibility

Gain and noise figure can be improved by minimizing the gate length, for this reason e-beam lithography was chosen for exposing 0.25 μm gate. The gate resistance and gate-source resistance also affect the gain and noise performance. Considerations were given to minimize these resistances [1]. An initial estimate of the equivalent circuit and noise parameters were made [1] using published equations. The resultant equivalent circuit model is shown in Figure 2-11 for 0.25 x 100 μm^2 FET. Figure 2-12 shows the gain and noise circles for such a FET at 29 GHz. The analysis of these devices showed the gain and noise figure specifications of the LNA could be met by such devices.

2.1.6 Overall Receiver

The functional configuration was shown in the previous section 1. The gain, noise figure, dc power consumption, overall noise and gain performance was shown in Figure 1-1 and Figure 1-2. Four submodules were interconnected on a single 3x9 mm^2 carrier plate to form the interconnected

receive module (Figure 2-13). Fin-line waveguide to microstrip transitions were used for LO and RF, the IF was taken through SMA by a 50 line. An important feature of this fixture is that the chip would be enclosed in a waveguide below cut-off. This provides an inherent RF shielding and good isolation between input and output.

2.2 Task II: Phase Shifter Fabrication and Evaluation

The objectives of this task were the following:

i) design, fabricate and test a 5-bit phase shifter, each bit $\pm$ 3° at the center band over 27.5-30 GHz;

ii) deliver 100 of these monolithic chips to NASA/LeRC

The efforts were started at the beginning of this task to select a proper technology which would be both reliable and reproducible. Two approaches were tested, one with power FET fabrication and the other with self aligned gate (SAG) fabrication technique. Two resonant FET switches configurations (shunt and series) were also tested. One bit 180° phase shifter was tested using shunt FETs; and a multibit (3 bit) phase shifter was also designed and tested with series FETs at the beginning of the program. Figure 2-14 shows the layout of a single bit 180° phase shifter. Figures 2-15, 2-16(a) and 2-16(b) show the measured insertion phase, rf test fixture (cover removed) and the measured insertion loss (including 1.4 dB fixture loss) respectively for one of these 180° bit chips. The SAG technology showed an encouraging trend for lowering the "ON" resistance below 8 ohms for 400 μm device. The "ON" resistance value was verified by modeling the measured phase shifter performance with the FET parameters. Figure 2-17 shows the multi-bit phase shifter (180°, 90°, and 45° bits switched line type and 22.5° bit loaded line type) and an enlarged view of the 90° phase shifter. The initial results for this multibit phase shifter is shown in [1].

Since two technologies were being developed (SAG and power FET), over multiple runs the power FET process proved as good as SAG in terms of low "ON" resistance ($\simeq$ 8 ohm) and showed a higher RF yield. So a final mask set was designed with the following main criteria in mind;

i) extension of loaded line phase shifter design to include the 5th 11.25° bit;

ii) inclusion of an on-chip bias tee circuit;

iii) provision in the mask set to include phase shifter fabrication by either SAG or power FET process to enhance the yield.

The fifth bit (11.25°) was incorporated in the same 22.5° loaded line bit by adjusting the gate voltage of the FETs from 0 to -5V in an analog fashion. Figure 2-18(a) shows the final layout of such a 5-bit phase shifter with bias Tees on-chip; Figure 2-18(b) shows the layout with four bias pads (no bias Tee's) as a back up design. The delivery run with these designs was implemented with power FET fabrication process having recessed gates. Eighty of the phase shifters (Figure 2-18(a)) were visually inspected, dc tested and delivered to NASA on June 10, 1985. Additionally, two phase shifter chips were rf tested and mounted on chip carriers and a third was similarly rf tested and mounted in the test fixture. These three chips along with a comprehensive set of rf and dc data taken from a total of five chips were also delivered. Prior to this delivery, twenty 3-bit phase shifter submodules including two rf tested ones and a test fixture with a mounted 3-bit phase shifter were delivered in October, 1984 [2]. These deliveries completed the phase shifter delivery requirement to NASA. Figure 2-19 shows the rf performance of the 5-bit phase shifter with on-chip bias (Figure 2-18(a)). Figure 2-20 shows the rf performance of the 5-bit phase shifter with backup approach. In the design of Figure 2-18(a), the insertion loss at the center of the band (30 GHz) was 8 ± 1.5 dB; the phase characteristics were broadband. The loaded line circuit provided 10-15° of additional shift instead of 22.5°. Because of this, the loaded line could not produce the additional 11.25° bit as predicted. So Figure 2-18(c) shows the results for 16 states. On the other hand, for the backup design of Figure 2-18(b), it was possible to produce the additional bit of 11.25° as shown in Figure 2-18(d). The responses shown in Figure 2-18(c) and 2-18(d) were typical of the phase shifter fabricated in the 9th and final run. The gate pad capacitance in the backup design (Figure 2-20) showed to have effect on the differential phase shift (page 7 of [2]). The gate loading was explained in [1] on the performance of the phase shifter.

2.3 Task III: Gain Control Amplifier Fabrication and Evaluation

The requirements for gain control submodule have been already discussed in Section 2.1.2. The mask for gain control contained the following three basic reticles:

(1) discrete dual gate FET,
(2) single and dual gate FETs with input matching,
(3) 2-stage dual gate amplifier.

These three basic element layouts are shown in Figure 2-19(a), (b), and (c). The discrete dual gate FET consisted of a $0.25 \times 100\ \mu m^2$ FET with two sets of fingers. The dual gate device had an on-chip MIM capacitor for RF grounding the control gate. The input matching circuits consisted of a high impedance transmission line with a grounded capacitor at one end. A picture of fabricated

dual gate FET is shown in Figure 2-20 along with the dc characteristics. The RF results on discrete dual gate FETs showed a gain of 10 dB at 30 GHz with a gain control ability (by varying the second gate voltage) of nearly 30 dB. It was also revealed that the device was unstable and the output reflection was greater than one. A closer look at the simulation showed the source of instability was due to a common ground used by the source and the second gate. Figure 2-21 shows the schematic of the old dual gate (unstable) along with the schematic of the new dual gate FET (stable); in the new layout the ground of source and the second gate was made separate. A new mask was created with the modified dual gate layout with 20 two-stage dual gate amplifiers per reticle. Besides these complete two-stage dual gate amplifiers, there were two versions of single stage dual gate amplifier for checking out the input and output matching circuits. Figure 2-22 shows all the layout for these three amplifiers. The new modified dual gate FET [2] layout is shown in Figure 2-23. The new final equivalent circuit for this device is shown in Figure 2-24. The schematic of the two stage amplifier is given in Figure 2-25. The final fabricated circuit was measured with some on-chip rf tuning as shown in Figure 2-26. The amplifier showed a gain of 12 dB at the center of the band 27.5-30 GHz (Figure 2-27). It had a gain of 12 dB at the center of the band and the 2 dB bandwidth was 2 GHz, slightly less than the design bandwidth of 2.5 GHz. The phase shift envelope was 20° at the center of the band and increased to approximately 45° at the band edge of 27.5 GHz, over the desired range of gain variation. The input return loss was less than 5 dB over most of the band and output return loss was poorer due to the high output impedance of the dual gate. The results were reported in 1987 symposium paper [3]. A total delivery of 100 chips was made at the end of this effort (47 chips were delivered at the end of second "best effort" iteration, and 53 chips delivered at the end of the third and final iteration). This was the first gain control circuit demonstration in Ka-band [4].

2.4 Task IV: RF/IF Submodule Fabrication Evaluation and Delivery

The main functions of this submodule are mentioned in 2.1.3. The submodule consisted of three parts, namely balanced Schottky diode mixer, IF amplifier and 22 GHz LO amplifier.

2.4.1 Mixer

Figure 2-28 shows the actual fabricated chip of the mixer with modified rat race hybrid. The circuit consisted of a rat race hybrid, two Schottky diodes, filters and signal ports. Figure 2-29 shows the RF signal and LO magnitude balance at the two diode ports. The diode area selection, resistance and capacitance calculations are given in an annual report [2, page 18]. Figure 2-30 shows the CALMA layout of ion-implanted mixer diode with 1 μm Schottky contacts for reducing

the contact resistance. It needs to be mentioned it was a first ever effort to develop a planar, ion implanted, FET-compatible mixer process using 3 inch wafers with direct step-on-wafer and optical projection lithography. Since two distinct device structures were needed in the RF/IF module (the local oscillator reference and IF amplifiers needed submicron FETs and the mixer needed high cutoff frequency Schottky mixer diodes), a flow chart of the process developed under HI IR&D programs is described in Figure 2-31. A detailed description can be found in [5]. The measured conversion loss for two mixer chips from the first iteration is shown in Figure 2-32. The loss went as high as 15 dB at some frequency in the band. This performance degradation was traced to the high VSWR at signal and local oscillator ports. The key reason for high VSWR was high diode junction resistance. The diode resistance after a series of measurements was found to be 300-400 instead of 115 (with which the mixer was designed) with 1.5 mA of rectified current. In the final design of mixer, the diodes had 21 one-micron dots connected by airbridge for minimum parasitic capacitance. A cross-sectional view of such a diode is shown in Figure 2-33. The measured I-V characteristics of such a diode is given in Figure 2-34. The zero bias junction capacitance was measured as .0517 pf and the "ON" series resistance was 5 Ω. The ideality factor was ~ 1.06. The final mixer layout is shown in Figure 2-35. Performance of such a mixer was evaluated with a 22 GHz oscillator source, the measured conversion loss vs. signal and IF frequency is shown in Figure 2-36 at a local oscillator power level of 13 dBm. The minimum conversion loss was found to occur at this local oscillator power level (Figure 2-37) over the band of interest. The mixers developed during this program demonstrated the following for the first time,

1) IF frequencies higher than any other completely planar microstrip mixer
2) ion implanted mixer diode cutoff frequencies beyond those any other diodes.

A total of 49 mixer chips were visually inspected, dc tested and delivered to NASA. One mounted mixer chip was also delivered along with those 49 chips.

2.4.2 IF Amplifier

The schematic for a single stage IF amplifier is shown in Figure 2-38. The corresponding layout is given in Figure 2-39. The calculated frequency response of the amplifier is shown in Figure 2-40. Due to process related problem, on-chip IF amplifiers did not function properly due to degraded FET characteristics. No delivery was made of IF amplifier.

2.4.3 22 GHz LO Amplifier

The amplifier was designed with 0.25 x 100 μm^2 gate FET. Figure 2-41 shows the schematic of the three stage amplifiers with the simulated gain characteristics. The circuit was checked with equivalent circuit parameter variation; it still showed reasonable gain (20 dB) at 22 GHz in the extreme case of more than 50% variation in Cgs and 30% variation in gm. A fabricated chip of this 3-stage amplifier is shown in Figure 2-42. The chip dimensions were approximately 2.3 x 0.8 x 0.15 mm^3. The measured gain vs. frequency characteristics are shown in Figure 2-43. Ten local oscillator amplifiers were delivered to NASA in 1987.

2.5 Task V: Low Noise Amplifiers

The discrete devices (MESFETs: 0.25 x 100 μm^2) were first characterized for gain and noise figure performance. A single gate FET with input matching circuit was also characterized. Two types of material were also examined, ion-implanted and VPE. Devices fabricated on ion-implanted material produced 8.2 dB gain with 3.4 dB noise figure at 17 GHz and 3.8 dB gain with 4.6 dB noise figure at 30 GHz. Devices on VPE material achieved 8.3 dB gain with 2.5 dB noise figure at 17 GHz. The s-parameters were also characterized. Figure 2-44 shows the measured S11 and S22 for 0.25 x 100 μm^2 ion implanted FETs. The devices fabricated on VPE material showed a higher input capacitance and higher transconductance than those for ion implanted devices. The total gain turned out to be the same for both ion-implanted and VPE devices. It was decided to follow ion implantation process for compatibility with other submodule fabrication. Based on the measurement of the discrete devices, an equivalent circuit was derived Figure 2-45 and four different low noise amplifier designs were made. They were:

LNAIA	A single stage amplifier based on the 0.25 x 100 μm^2 FETs
LNAIB	A single stage amplifier with different input and output matching networks than LNAIA
LNA2A	A two-stage amplifier based on 0.25 x 100 μm^2 gate FETs
LNA2B	A two-stage amplifier with different matching networks than LNA2A.

Figure 2-46 shows all these four layouts for the amplifiers. The two stage LNA was to serve as a building block for the 32 dB "front-end" LNA. The chip size for two-stage LNAs was 2.3 x 0.71 x 0.15 mm^3.

The final circuit (LNA2B) was measured with on-chip modification as shown in Figure 2-47. The response before and after the modification are shown in Figure 2-48. A total of ten unmodified two-stage LNA was delivered to NASA. A modified version of the LNA was used in the receive module delivered to NASA. The low gain of the LNA caused a high overall noise figure for the receive module.

2.6 Task VI: Interconnect Receive Module Design

The submodule performance goals as well as performance goals of the interconnect receiver are summarized in Figure 2-49. The interconnected receive module was to consist of four monolithic chips, the low noise amplifier, phase shifter, gain control amplifier and the RF/IF downconverter. The receiver was to have a conversion gain around 30 dB with an overall noise figure of 5.0 dB. The gain control amplifier had an adjustable continuous gain control from -1 dB to 12 dB. A 5-bit phase shifter was used for phase control. To demonstrate the 30 GHz receiver with existing IC's, a preliminary version of the receiver was assembled and demonstrated with three chips, a two stage LNA, a two stage gain control amplifier, and a phase shifter. These chips were individually tested to screen out RF bad chips before being interconnected. Fig. 2-50 shows the chips in a single housing having standard waveguide input and output ports. The dc blocking between chips and simple bias filtering were achieved on quartz substrates (Fig. 2-51). The RF testing of the interconnected receive module included gain/loss measurements, relative phase shift measurements and noise figure measurement. A full set of measurement data was delivered to NASA at the time of actual demonstration of the receiver at the NASA/LeRC. The data are also given in appendix B of [5]. Figure 2-52 shows the gain vs. frequency characteristics for the receive module at five gain settings across the band 27.5-30 GHz. The corresponding relative phase shift is shown in Figure 2-53. Worst case phase envelope for the five different settings was $\pm$ 12° at the band edges Figure 2-54 shows the relative insertion phase characteristics as the phase shifter chip was cycled through sixteen states. Nearly full 360° coverage was obtained a the upper band edge, while reduced coverage of about 310-320° was obtained in the lower half of the band. Finally, in Figure 2-55, the insertion gain envelope is plotted for all the sixteen states. It is $\pm$ 2 dB over the whole band. Noise figure data was taken at center band for the nominal gain settings of + 12, 9, 6, 2, and -1 dB. Table 2-1 shows the data. The best noise figure of 14 dB was obtained at the maximum gain setting of 12 dB. Three such interconnected receiver modules were delivered during the program period.

2.7 Task VII: Monolithic CTS Receiver Development

The goal for this task was to integrate monolithically the front end RF submodules (LNA, phase shifter and the GCA). To accomplish this on a single chip, the phase shifter size had to be reduced significantly. A six-stage LNA had to be incorporated also to increase the front-end gain. An initial mask with the following items was generated.

- A reduced size 5-bit phase shifter
- A two-stage LNA
- Digital control circuits
- Four and six stage LNAs
- Test FETs and circuits

The first three items above were a combined layout representing a single monolithic IC, and the last two were separate ICs. Figure 2-56 shows the reticle layout for the whole mask. The designs were based on 4 mil GaAs substrate. The design philosophy of designing four and six stage LNAs are given on page 73 of [5]. Figure 2-57 shows the LNA/phase shifter IC consisting of a reduced size 5-bit phase shifter.

Fabrication of this CTS receiver mask started in 1987. The process involved multiple implants for the phase shifter switches, logic FETs and LNA FETs. In addition, the gate level process steps were carried out separately for each device, because of difference in gate lengths and recess etch depths. The receiver fabrication used a hybrid lithography process with direct-step-on-wafer optical exposure for all levels except the LNA gate which was exposed by E-beam direct writing in a multilayer resist. The fabrication was on full 3" wafers. During fabrication of this complex mask, a few process related problems were detected [5] and corrected. Working phase shifters with on-chip logic were fabricated and demonstrated. The new phase shifters had two significant features:

- The size was reduced from 2.5 x 5.5 x 0.15 mm^3 to 3.2 x 2.7 x 0.15 mm^3.
- On-chip implanted resistors were used to improve the RF decoupling.

The phase shifter was evaluated both in NASA band (Fig. 2-58) as well as in the best frequency range of operation (Figure 2-59). Figure 2-60 and 2-61 show the insertion loss envelope for these two bands. Even through the total overall insertion loss was high, the insertion loss envelope was reduced substantially (nearly $\pm$ 0.5 dB at the high end, Figure 2-60). The new phase shifter design also included 2 on-chip logic circuits with two different designs. A photograph of these logic circuits is shown in Figure 2-62(a). To demonstrate the logic control of bits, one 180° bit was connected with bondwire to a logic control circuit. The phase and insertion loss characteristics with 180° bit are shown in Figure 20-62(b) and 2-62(c) respectively. The characteristics were similar to those measured earlier with the following exceptions:

- The insertion loss was slightly higher.
- The insertion loss envelope was broader at the lower end of the frequency range.

The higher insertion loss could be partly due to the addition of dc blocks, which would keep the transmission lines in the phase shifter floating at 6 volt for the control logic. During fabrication of the CTS receiver with corrected set of masks, a few other process related problems appeared. They have been discussed in [6]. One more circuit, 2-stage LNA was tested for DC and RF performance. The layout of such an amplifier on 4-mil substrate is shown in Figure 2-63. Figure 2-64 shows the gain and noise figure performance of a 2-stage amplifier. The best performance achieved was 7.0 dB noise figure with 6.1 dB gain at 28.5 GHz. Gain and return loss data over full NASA band is shown in Figure 2-65. RF characteristics of phase shifter were also measured from the same wafer. The characteristics shown in Figure 2-66 for insertion loss and Figure 2-67 for phase response were taken after cutting the control lines at the crossover points as shown in Figure 2-68. By reducing the coupling between dc control lines and the RF line, the phase shifter performance improved; it shows lower insertion loss and tighter loss envelope.

The circuits, 2-stage LNA and phase shifters, so far reported in this subsection from CTS receiver fabrication did not involve any backside via-hole process. After completion of backside process on several wafers, a few 2-stage LNA's were selected for evaluation. The 2-stage LNAs used via-holes and SI_3N_4 capacitors. The LNAs did not show any gain in NASA's band of interest. 50 dc tested IC's (including 2-stage LNAs, 4-stage LNAs, 6-stage LNAs and phase shifters) were delivered to NASA at the end of this effort. Due to funding reductions in the program, the second and third iteration designs could not be completed as was originally planned at the beginning of this program [7].

2.8 Task VIII: Technology Assessment

The objective of this task was to report all the results on Honeywell technology during our program and compare these with the results reported in the technical literature. It was an ongoing task. A technology assessment report was issued at the end of all the tasks (I-VII) in April 1988 [8]. It compared all the key technology items developed during this program with the performance data available in the literature.

2.9 Task IX: Product Assurance

A product assurance program was implemented in accordance with the requirements of section 3.4 of the RFP. Log books concerning device and circuit development and fabrication were maintained from the outset of the program.

2.10 Task X: Reporting

Reports included updated work plans, monthly/bimonthly and annual technical progress reports, as well as monthly and quarterly financial and management reports.

2.11 Task XI: Phase Shifter Development for JPL/NASA

This task was started as an additional program to develop a 4-bit phase shifter for 31-33 GHz under the direction of NASA/LeRC and NASA/JPL.

We developed two types of phase shifters. The phase shifters are shown in Figure 2-69 and Figure 2-70. The first one (Figure 2-69) had three switched line type phase bits (180°, 90°, and 45°) and one loaded line type (22.5°). The second one (Figure 2-70) had three modified switched line bits (180°, 90;°, and 45°) and one loaded line bit (22.5°). The purpose of the second design was to lower the total insertion loss, while the first design had higher loss but conservative design. The modified switched line had FETs resonating at different frequencies. Figure 2-71 shows the difference of 90° bits between the conventional switched line approach and the modified switched line approach. The modified approach had two resonating FETs in the two branches (branch 1 and branch 2), while the conventional one had all the FETs resonating at one frequency (in this case center of the band, 32 GHz). Figure 2-72 shows the modeling of branch #1 FETs with measured data. It also shows a comparison of different models; one case the total junction inductance is evenly split, and the other case is with MTEE model available in CAD tool "LIBRA". The resonant frequencies calculated using these latter methods were quite off the target frequencies. This shift in in resonance frequencies affect both the insertion loss and phase of the bit. So it is required to design the loops properly to set the resonant frequencies right. Figure 2-73 shows the branch #2 FET model. As may be noted, the FETs in two branches were resonant at two different frequencies (35 GHz and 21 GHz). Figure 2-74 shows for example the difference in the calculated insertion loss of two approaches for the 45° bit. Figure 2-75 shows the measured performance (insertion loss) of these two phase shifters. The modified switched line design performed best over 32-33 GHz; the main reason was right angle bend discontinuities (which were used at freedom in this design) were not properly modeled by CAD tool "LIBRA". The transmission phase (< S21) of the right angle bends seemed to have discrepancy between the CAD model and the measured value. When the load line bit 22.5° in the new design was set "OFF" (note the bit was still connected in series with remaining three bits); the resulting measured response is shown in Figure 2-75. The response shows, the modified switched line approach gives a lower loss of 1.5-2dB than the conventional approach. When the loaded line bit was turned on, the loss went to

8 dB (from 5 to 6.5 dB). On the other hand the insertion loss for the switched line case remained between 7 and 9 dB over 31-33 GHz range for 16 states. Figure 2-76 shows the phase response of the two types. As mentioned earlier, because of suspected discrepancies in the right angle bend model of the CAD tool "LIBRA" the phase errors were higher in modified switched line circuit. A lot of right angle bends were used in the new design. Figure 2-77 shows the reflection at port 1 (180° bit side). The reflection on the loaded line side went down to -7 dB in the worst case for both types of designs. Both types have been checked with 0.5W of power, there was no noticeable degradation in any of the performances. At the end of the program, we delivered eighty-five rf functional chips of the conventional switched line design to NASA/LeRC and NASA/JPL. In the final review, we also strongly suggested a size reduction (by 30% approximately) and further reduction in insertion loss by going for a different topology and using 0.25 μm gate length for the device. In the whole program, we developed phase shifters using 1 μm gate length only. A gate length of 0.25 μm will reduce the "ON" resistance by a factor of two minimum. By changing the 4-bit topology from the present one loaded line bit (22.5°) and three switched line bits (180°, 90°, and 45°) to one loaded line bit (22.5°) and three reflective type bits (180°, 90°, and 45°) one could easily achieve the size reduction of approximately 30%; the latter topology will also cut down on the number of switching FETs from seven pairs to four pairs only. This would significantly improve the yield factor. By going for the latter topology and 0.25 μm gate length, one could, in effect, achieve the following:

i) reduced size
ii) higher yield
iii) lower insertion loss

All the above are considered very important from the system level integration point of view.

3.0 Program Conclusion and Recommendation

The program, during its course, demonstrated the viability of ion implantation technology in Ka-band; the technology allows easy integration of different components required in receiver technology. The program has given rise to the possibility of integrating the whole receiver in one MMIC. The level of integration may to some extent be decided by the performance compromise. Even though, not fully implemented in this program, a functional integrated receiver should be the next step. At the end of this program, along side MIMIC Phase 1 (funded by LABCOM) we have already measured far improved performance for ion implanted 0.25 μm device [9]. The three stage low noise amplifiers have shown 15 dB gain with 3.8 dB noise figure at 35 GHz. We also suggest a size reduction in the individual chips by adopting a better topology, this will make it easier to integrate the chip with phased arrays.

Reference

1. V. Sokolov, J. Geddes, P. Bauhahn, "30 GHz Monolithic Receive Module First Annual Report for Period Nov. 3, 1982-Oct. 31, 1983", Contract No. NAS3-23356.

2. P. Bauhahn, C. Chao, J. Geddes, V. Sokolov, "30 GHz Monolithic Module Third Annual Report for period Nov. 3., 1984-Oct. 31", 1985, Contract No. NAS3-23356.

3. V. Sokolov, J. Geddes, T. Contolatis, "Two-Stage Dual Gate MESFET Monolithic Gain Control Amplifier for Ka-Band", IEEE Microwave and Millimeter Wave Monolithic Circuits Symposium Digest, 1987, pp. 75-79.

4. J. Geddes, V. Sokolov, T. Contolatis, "Ka-Band Monolithic Gain Control Amplifier", Electronics Letters, Vol. 22, No. 9, pp. 503-504, April 24, 2986.

5. P. Bauhahn, J. Geddes, V. Sokolov, T. Contolatis, "30 GHz Monolithic Receive Module Interim Report for Period Nov. 1, 1985-Oct. 31, 1987", Contract # NAS3-23356.

6. J. Geddes, J. Mondal, T. Contolatis, V. Sokolov, "30 GHz Monolithic Receive Module, Annual Report Covering Nov. 1, 1987-Oct. 31, 1988", Contract # NAS3-23356.

7. J. Geddes, J. Mondal, T. Contolatis, V. Sokolov, "30 GHz Monolithic Receive Module Annual Report Covering Nov. 1, 1989-Oct. 31, 1988", Contract # NAS3-23356.

8. J. Geddes, let. al. "30 GHz Monolithic Receive Module Technology Assessment", April 1988, NASA Contract # NAS3-23356.

9. J. Mondal, J. Detry, J. Geddes, D. Carlson, "High Performance and High Yield Ka-Band Low Noise MMIC Using 0.25 μm Ion Implanted MESFET", submitted to Electron Device Letters.

10. W. Kellner et. al., "Design Consideration for Planar Schottky Barrier Diodes", Solid State Electronics, 23, pp. 9-15, Jan. 1980.

Further publications on this work:

1. P. Bauhahn, A. Contolatis, V. Sokolov, and C. Chao, "30 GHz Monolithic Balanced Mixers Using an Ion-Implanted FET-Compatible 3 inch GaAs Wafer Process Technology", 1986 IEEE Monolithic Circuits Symposium, pp. 45-50.

2. J. Geddes, V. Sokolov, D. Carlson, P. Bauhahn, and R. Ramanofsky, "Characteristics of 30 GHz MMIC Receivers for Satellite Feed Array Application", 1987 GaAs IC Symposium Technical Digest, pp. 155-158.

3. V. Sokolov, J. Geddes, T. Contolatis, and C. Chao, "A Ka-Band GaAs Monolithic Phase Shifter", IEEE Transactions on Electron Devices, Vol. ED-30, No. 12, lpp. 1855-1861, December 1983.

4. V. Sokolov, J. Geddes, T. Contolatis, and C. Chao, "A GaAs Monolithic Phase Shifter for 30 GHz Application", presented at the 1983 IEEE Microwave and Millimeter Wave Monolithic Circuits Symposium, Boston, MA, May 1983.

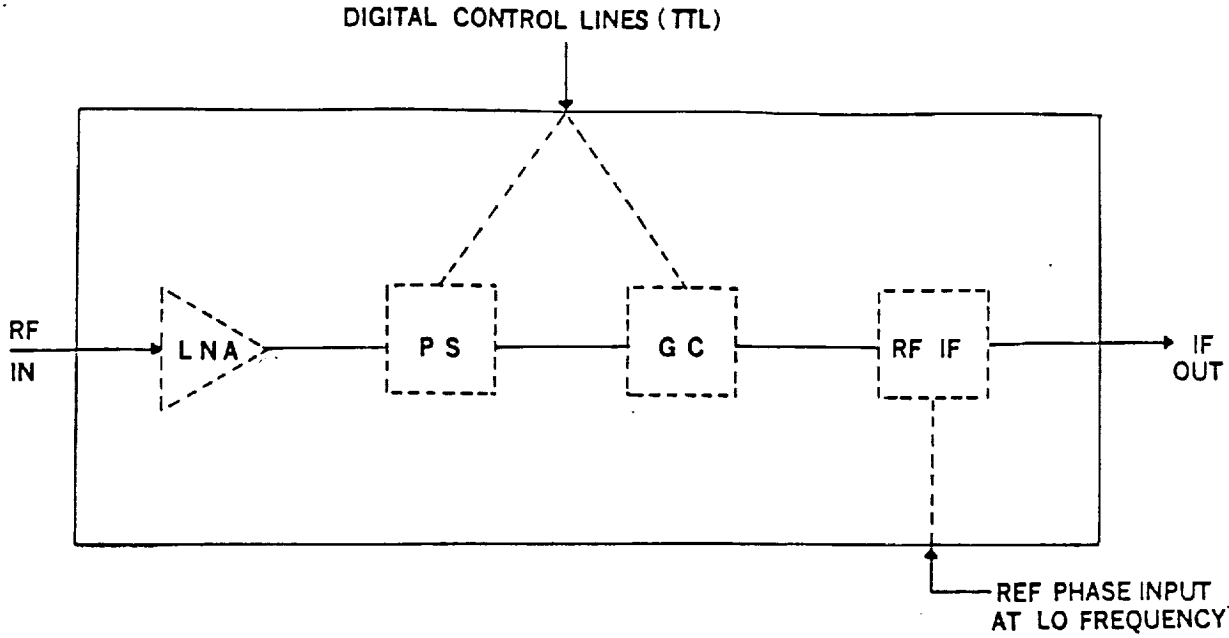


Figure 1-1 Submodule functions of receive module.

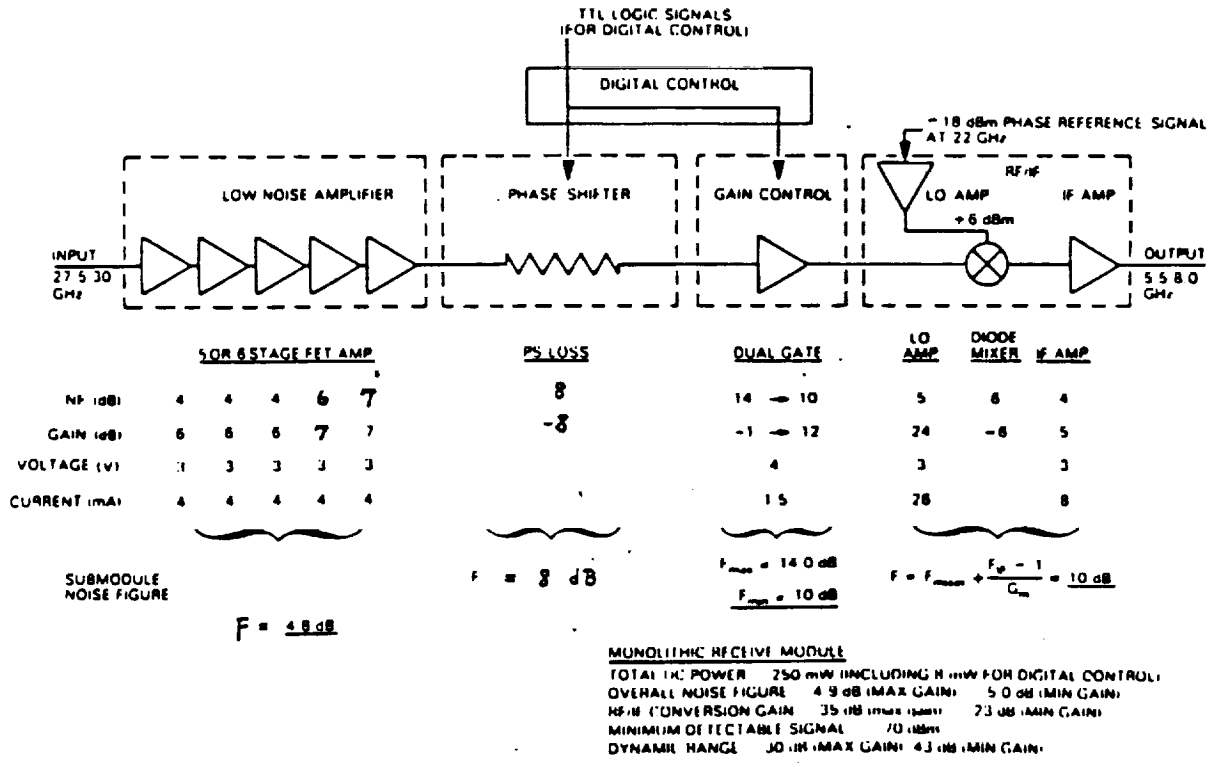


Figure 1-2 Block diagram of overall monolithic receiver.

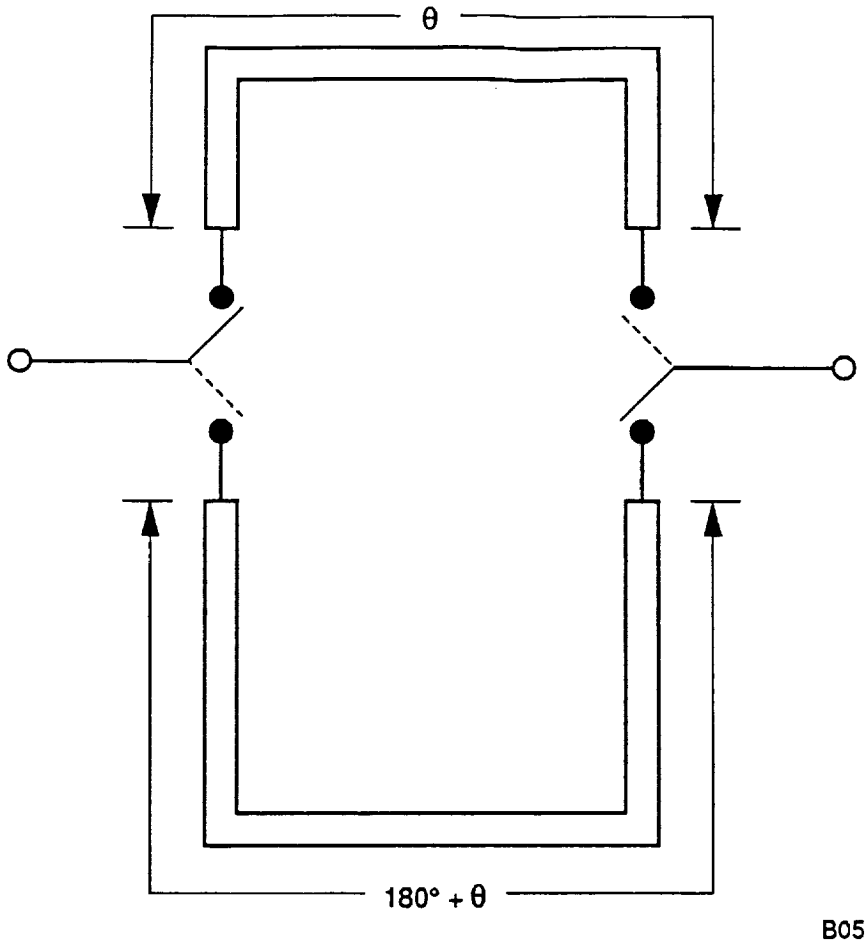


Figure 2-1(a) Schematic of 180° bit with switched lines.

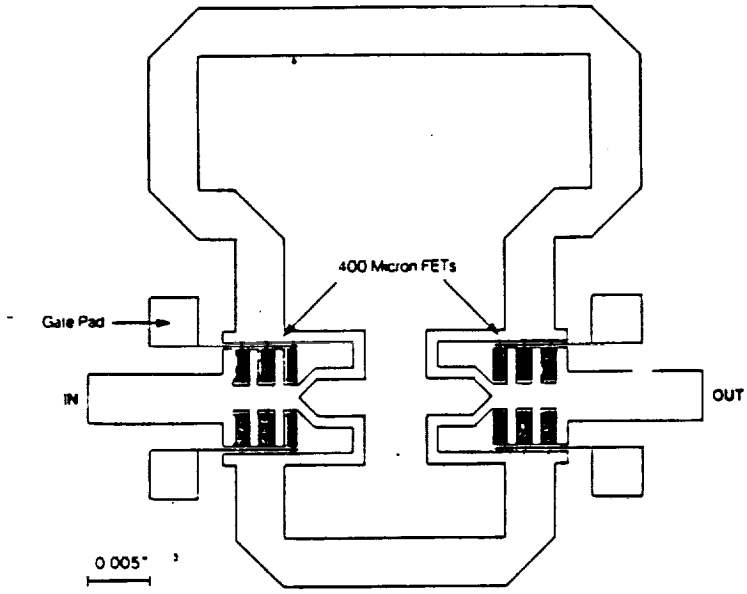


Figure 2-1(b) Layout of 180° bit using four series FET switches.

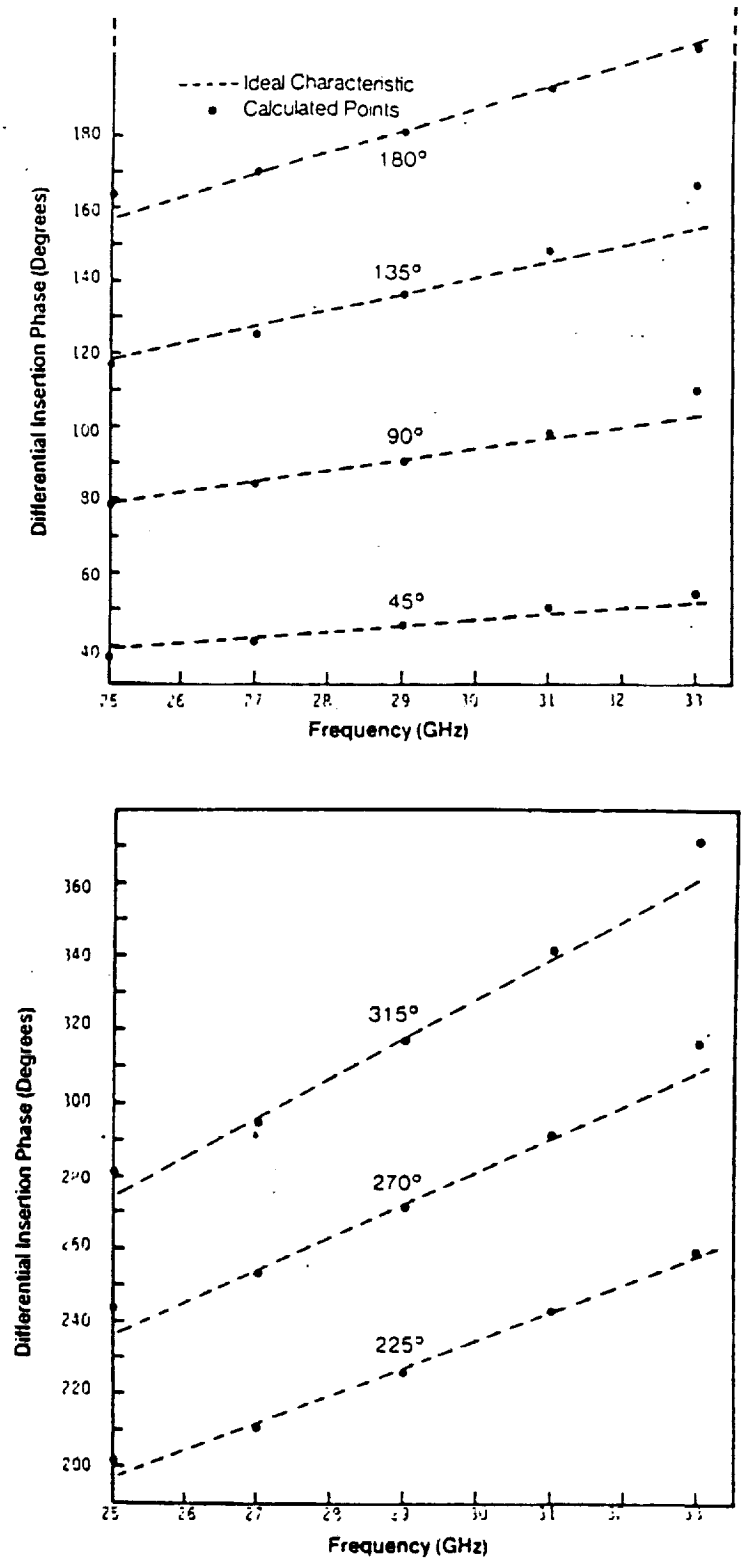


Figure 2-2 Calculated differential insertion phase for 3-bit phase shifter (180°, 90°, and 45°) using series FET switches.

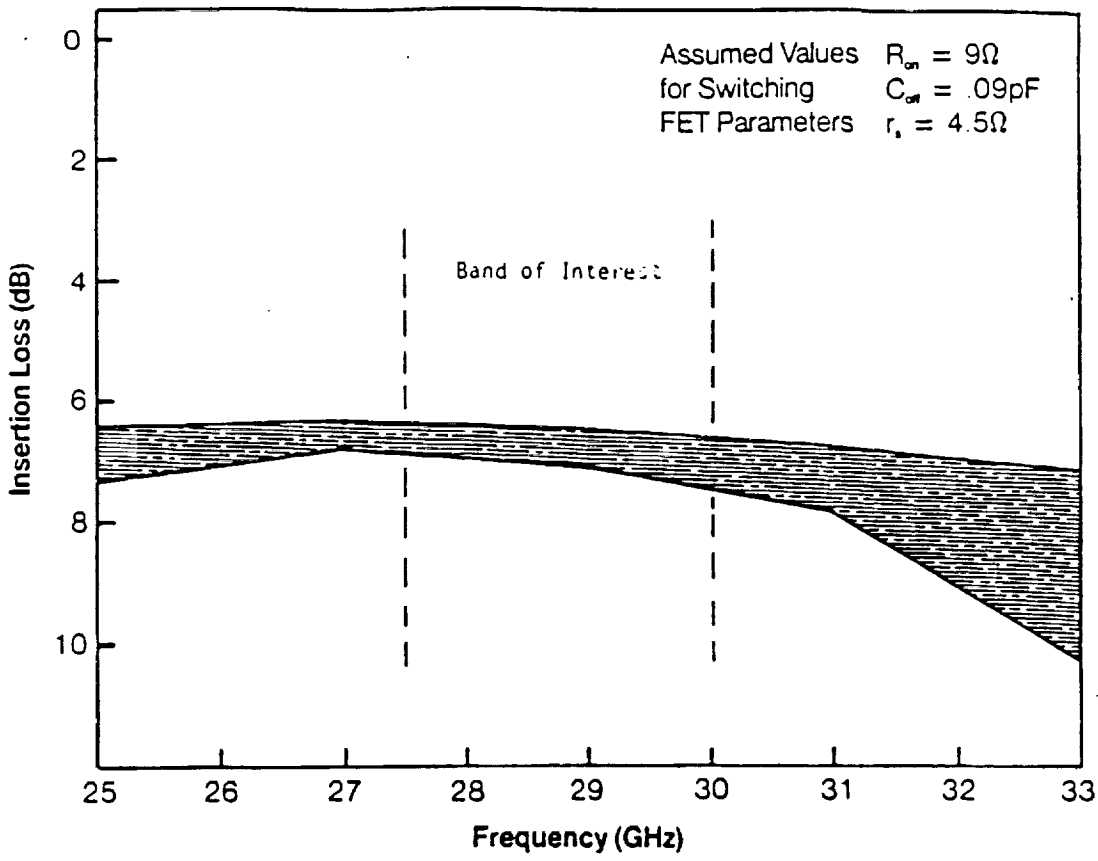
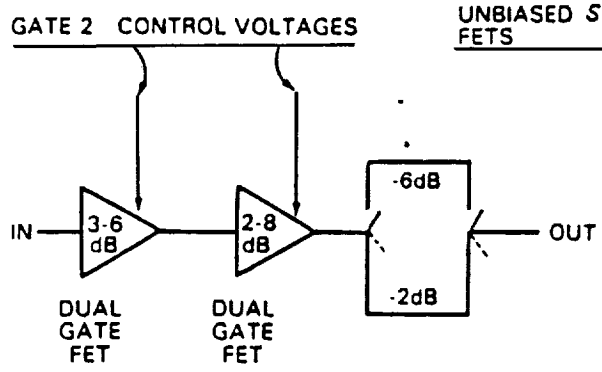


Figure 2-3 Calculated insertion loss envelope for eight states of 3-bit phase shifter



GAIN STATES (dB)	(G_1) 3,6	(G_2) 2,5,8
ASSOCIATED NOISE FIGURE (dB)	(F_1) 10,9	(F_2) 14,10,10
VOLTAGE(V)	4	4
MAX. CURRENT (mA)		8

	OVERALL GAIN STATES (dB)	CORRESPONDING RECEIVER RF/IF GAIN (dB)
①	3 + 2 − 6 = −1	17
②	3 + 5 − 6 = +2	20
③	3 + 5 − 2 = +6	24
④	6 + 5 − 2 = +9	27
⑤	6 + 8 − 2 = +12	30
⑥	−15 −15 − 6 = −36	OFF

WORST CASE NOISE FIGURE (STATE ①)

$$F_{MAX} = F_1 + \frac{F_2 - 1}{G_1} + \frac{L - 1}{G_1 G_2} = 13.6\text{dB}$$

BEST CASE NOISE FIGURE (STATE ⑤)

F_{MIN} = 10.1

Figure 2-4 Gain control scheme.

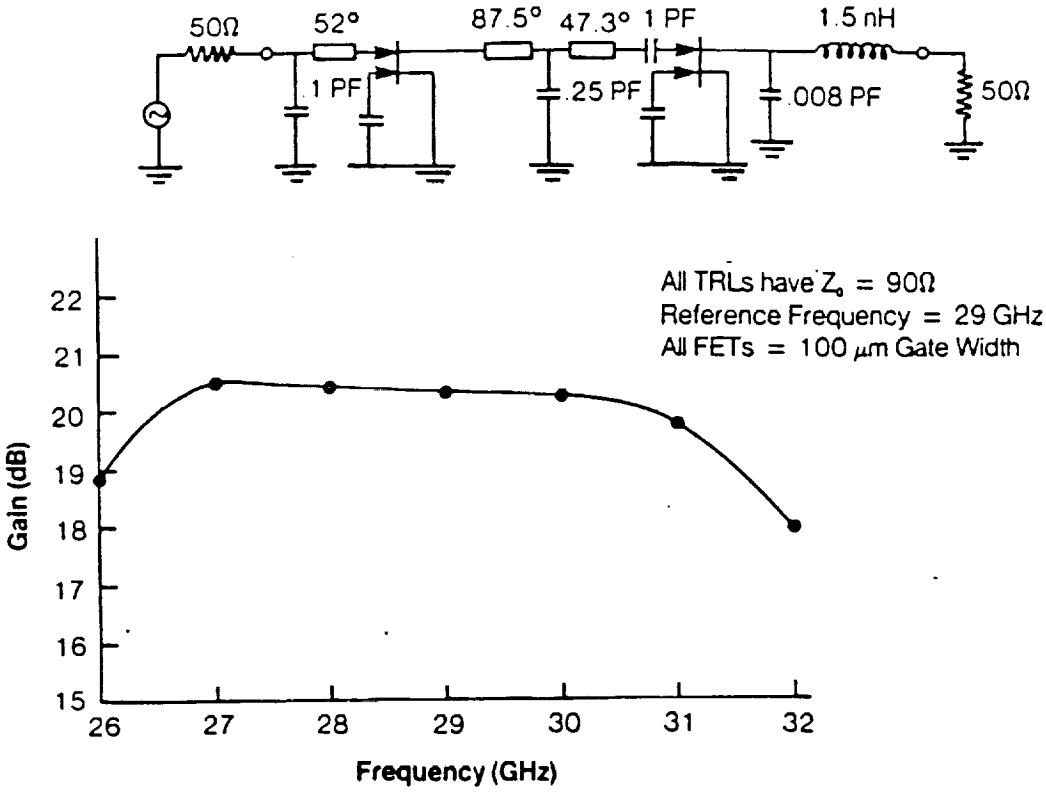


Figure 2-5 Circuit schematic and computer optimized response of a two-stage dual-gate FET amplifier.

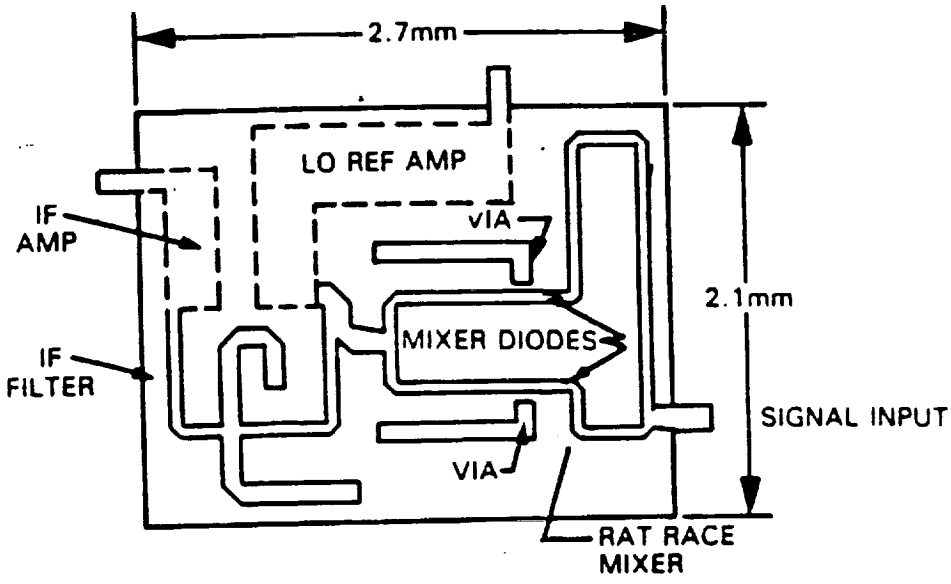


Figure 2-6 RF/IF submodule with RAT RACE hybrid.

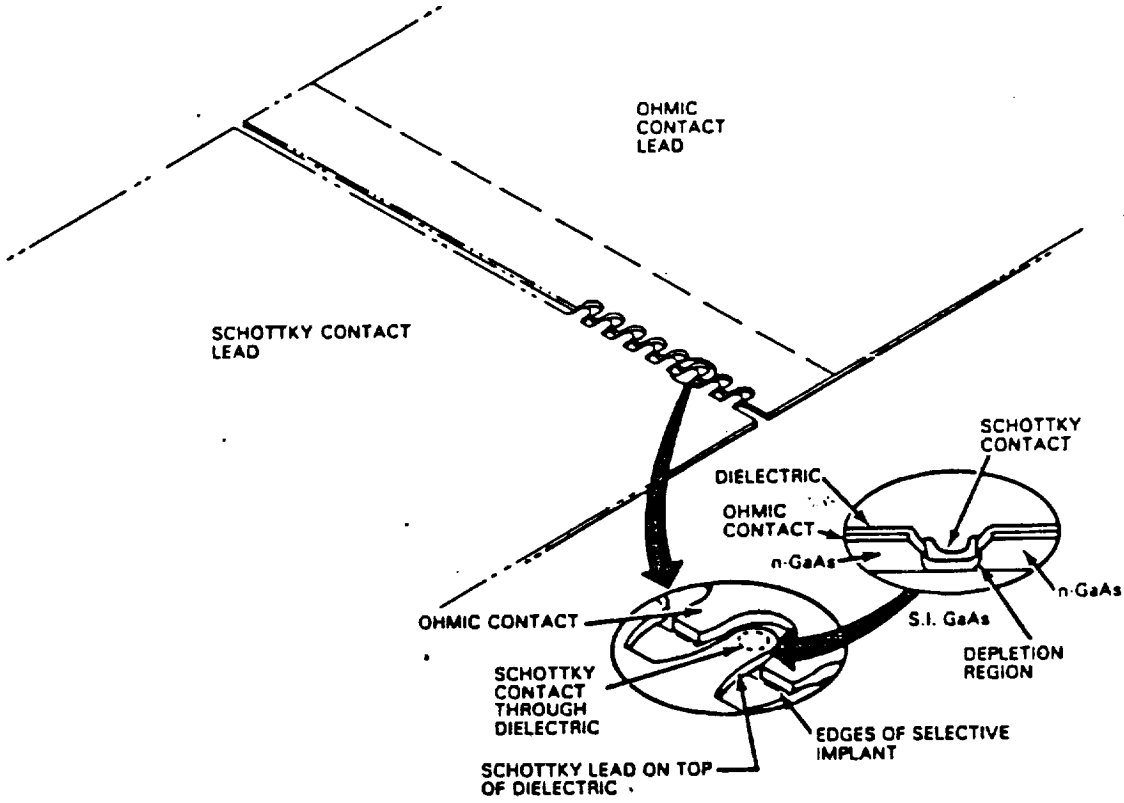


Figure 2-7 Diode structure for high mixer performance.

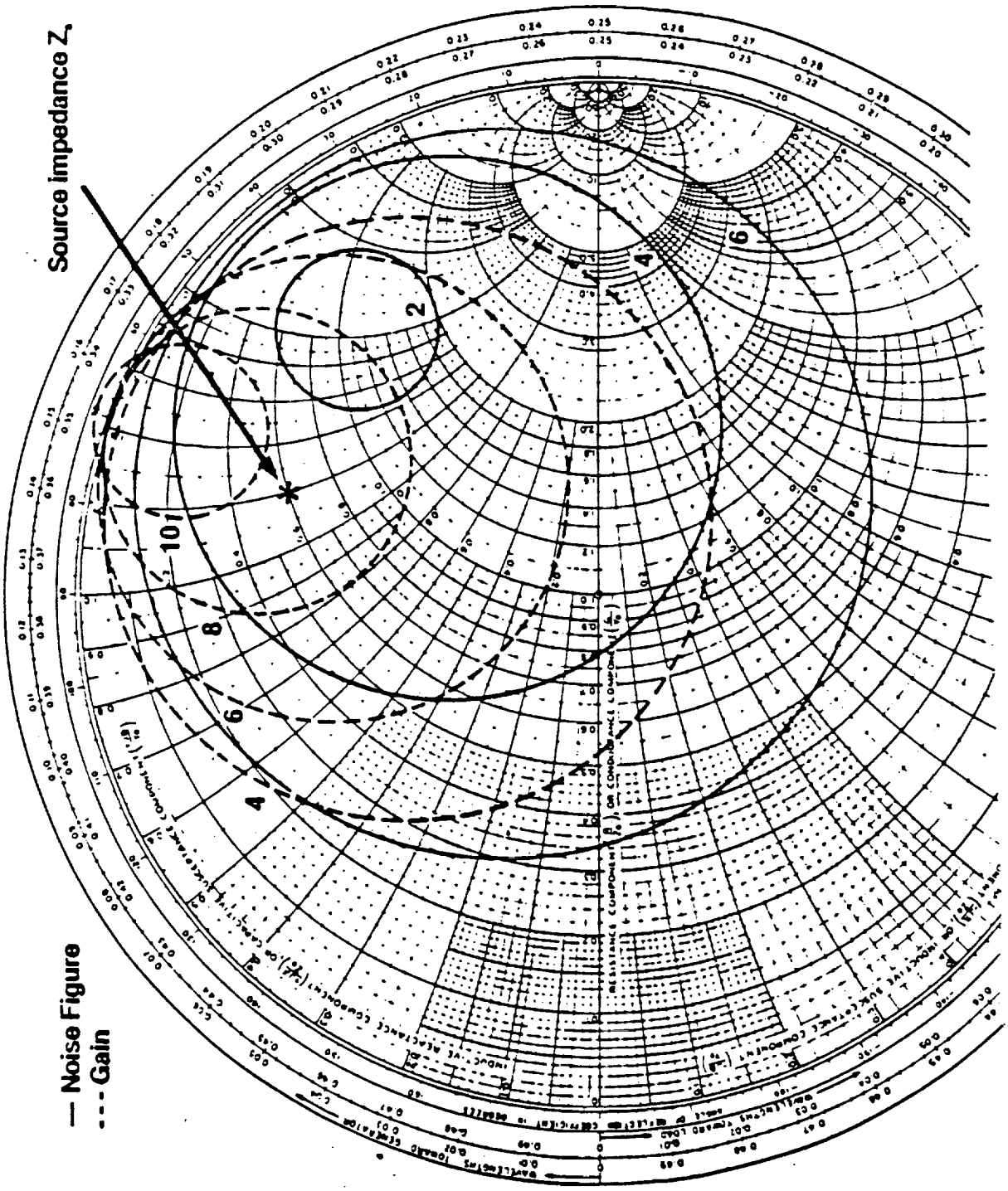


Figure 2-8 Gain and noise figure circles for 100 μm FET at 22 GHz.

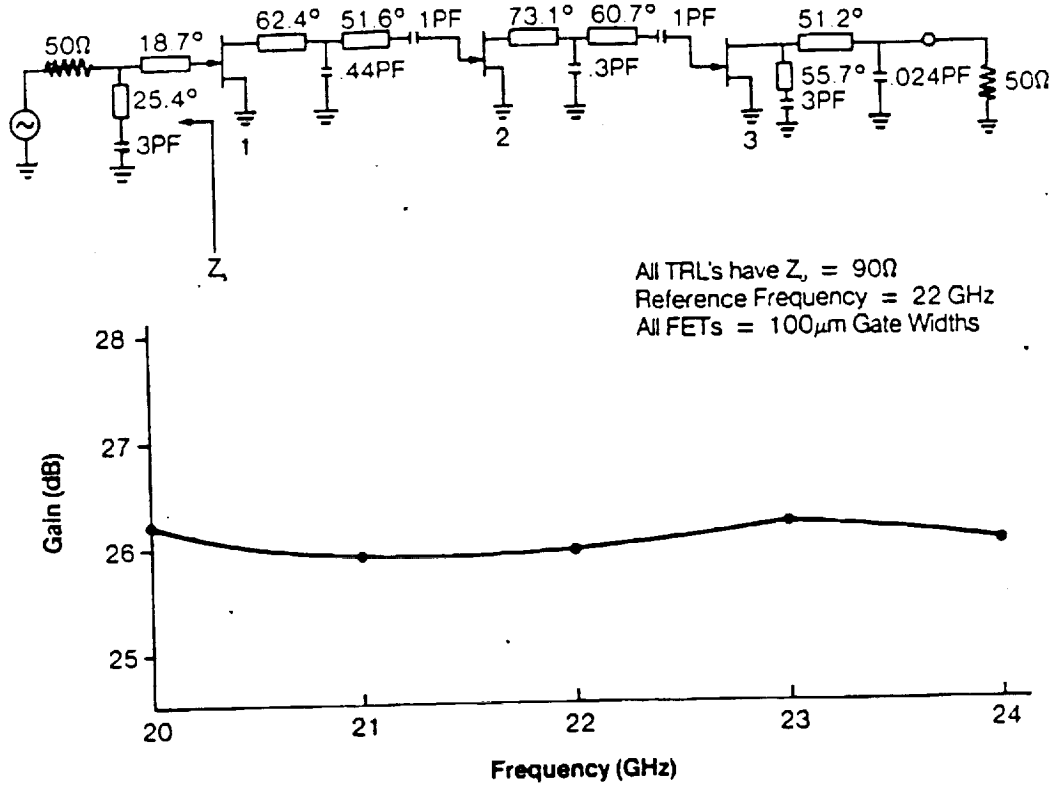


Figure 2-9 Three stage 22 GHz LO amplifier schematic and calculated response.

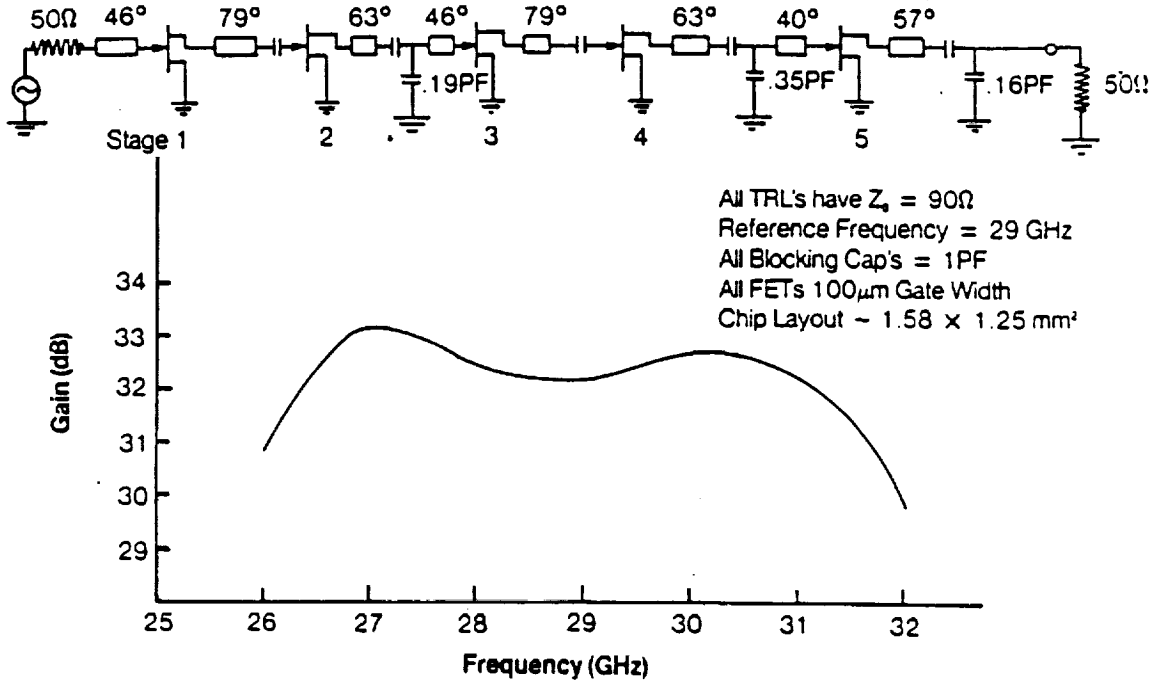
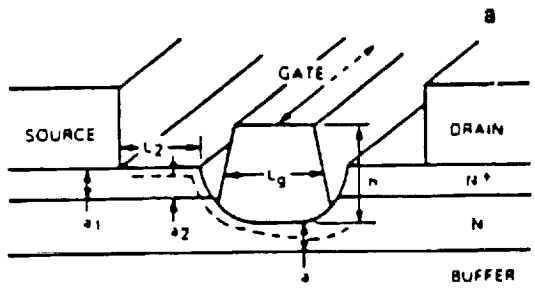


Figure 2-10 Initial 5-stage LNA design and response.



Gate length	L_g	= 0.25 microns
Unit gate width	w	= 50 microns
Channel thickness	a	= 0.15 microns
Doping density	N	= 2.5×10^{17}
Total gate width	Z	= 100 microns
Gate-source spacing	L_{sg}	= .75 microns
Gate metal thickness	h	= 0.5 microns
Specific contact resistance	r_c	= 10^{-6} ohm-cm^2
	a_1	= 0.22
	a_2	= 0.15
	N_1	= 2.5×10^{17}
	N_2	= 2.5×10^{17}

Calculated noise figure = 2.5 dB at 32 GHz

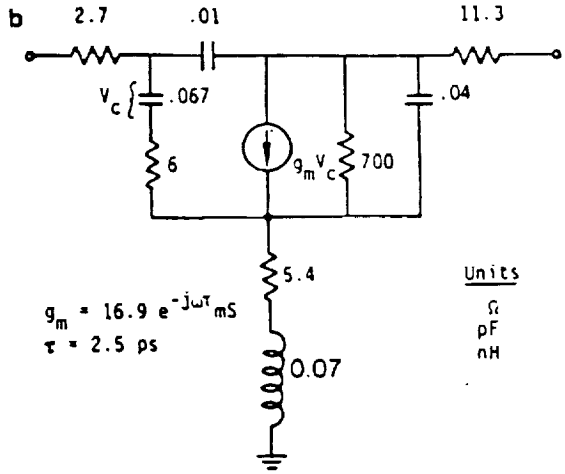


Figure 2-11 Device dimensions and estimated equivalent circuit of a 0.25 x 100 μm^2 FET.

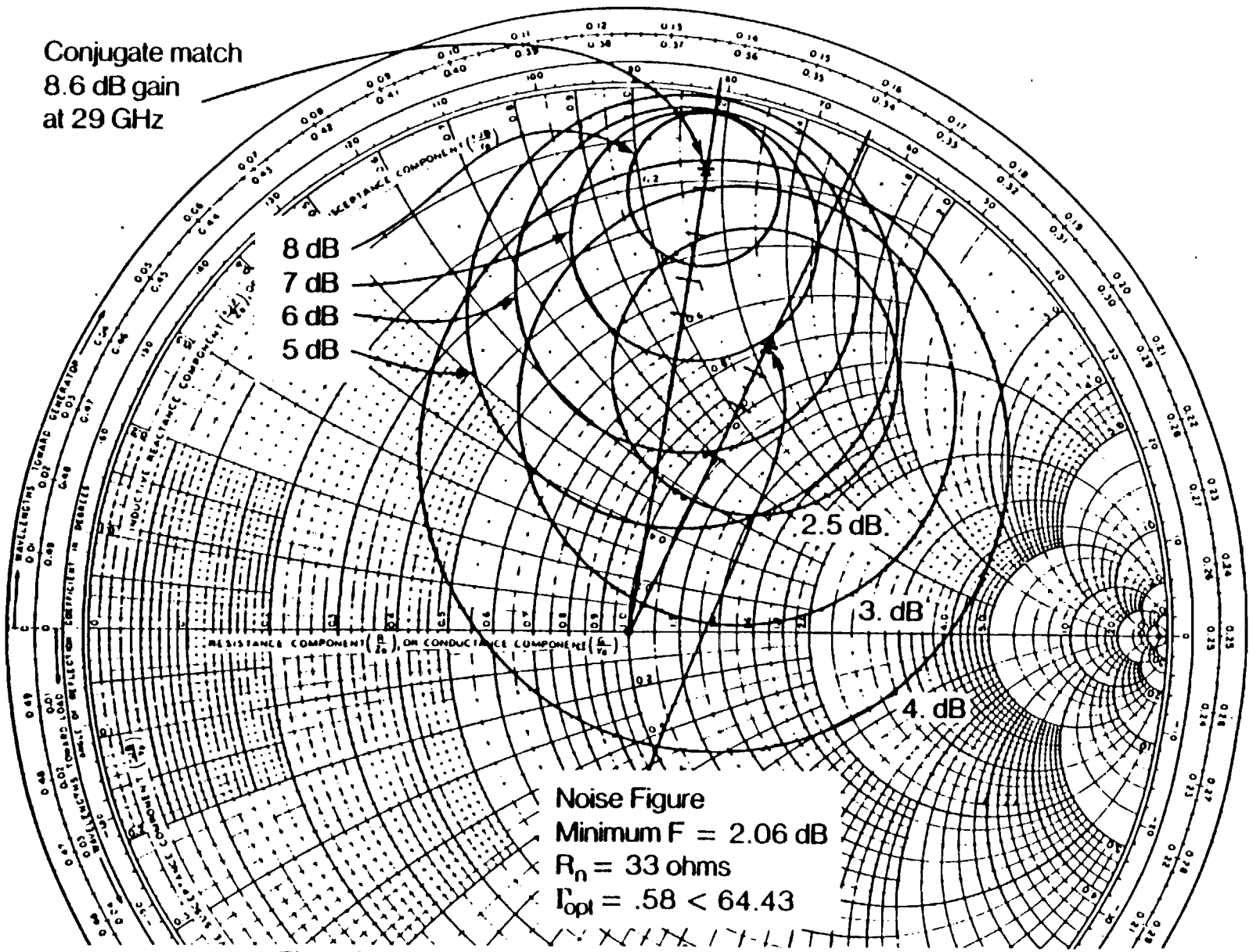


Figure 2-12 Gain and noise figure circles in the input plane of such a device at 29 GHz.

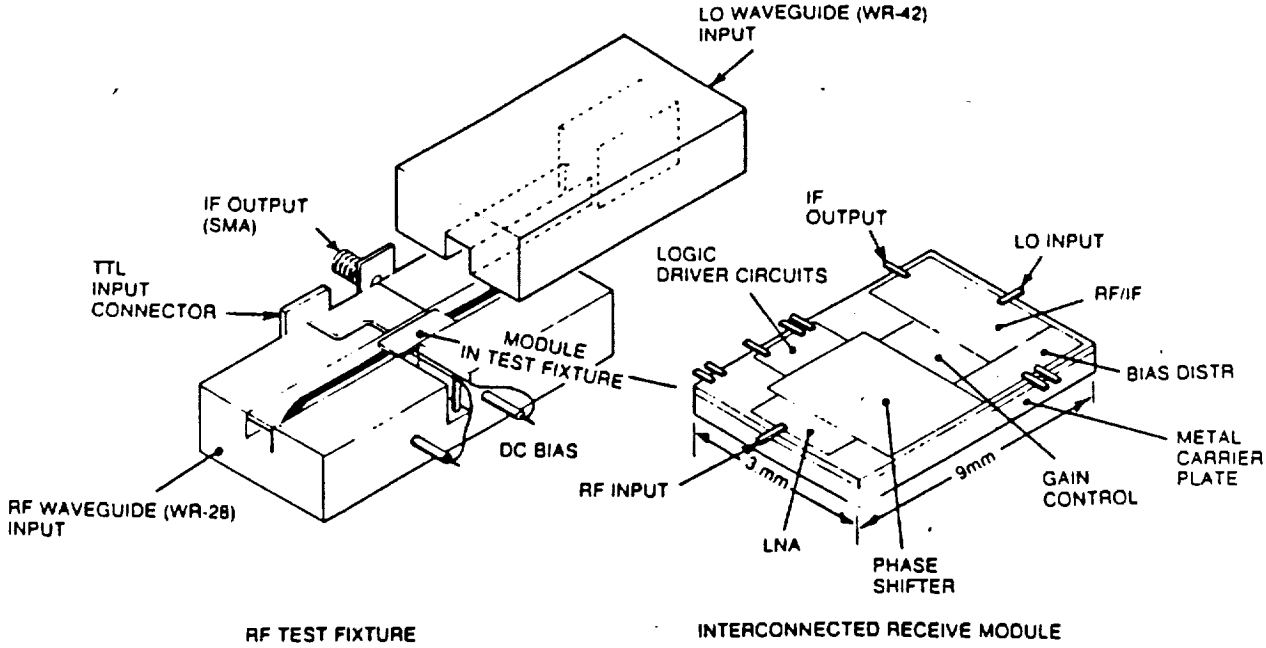


Figure 2-13 Interconnected receive module.

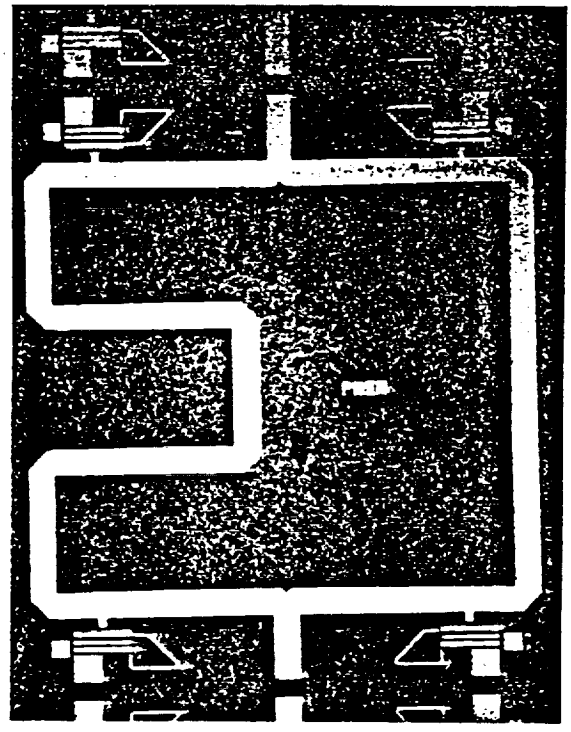
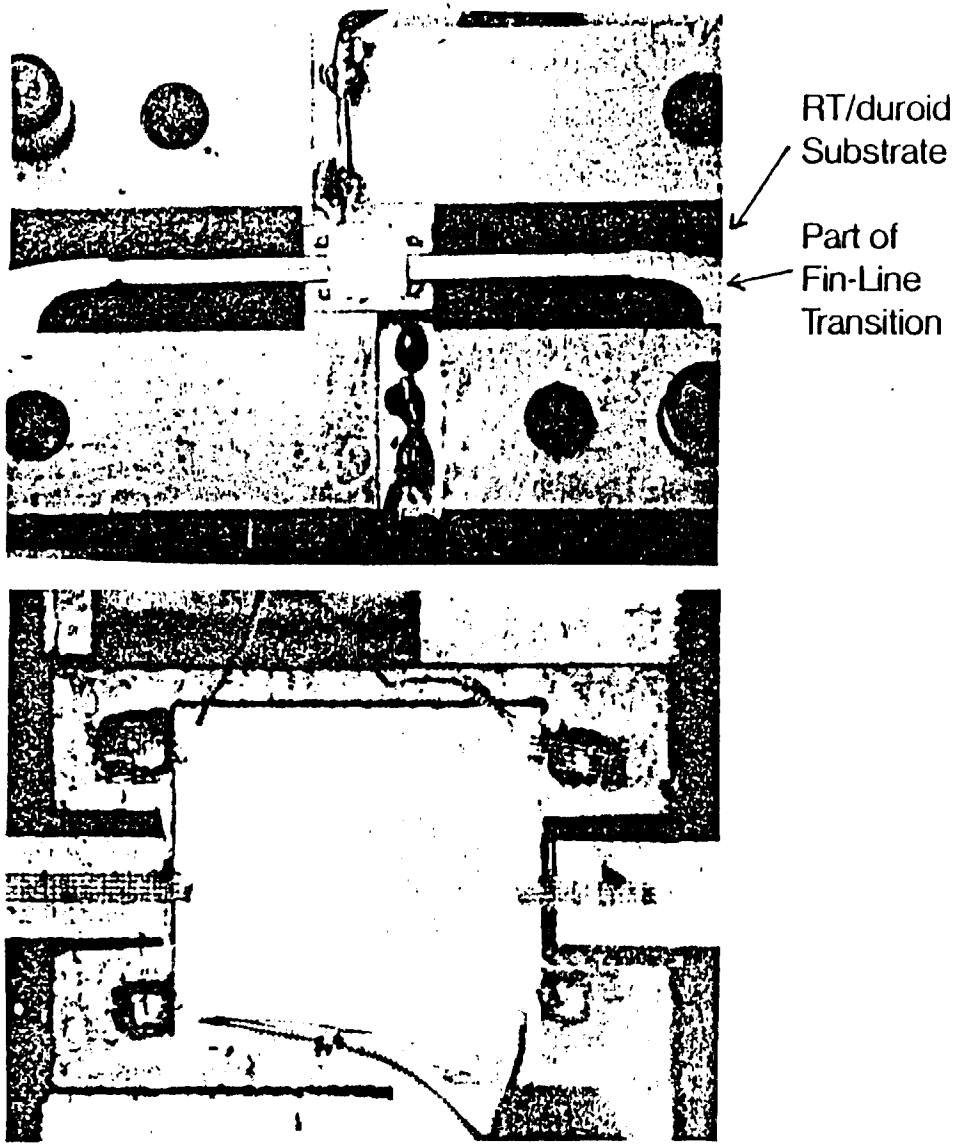


Figure 2-14 Chip picture of 180° phase bit using shunt FETs.



(Test Fixture and Chip)

Figure 2-16 (a) Test fixture.

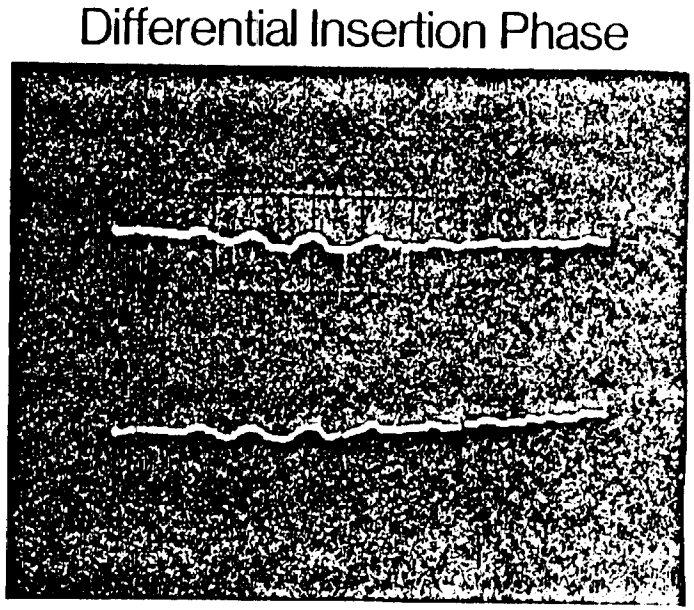
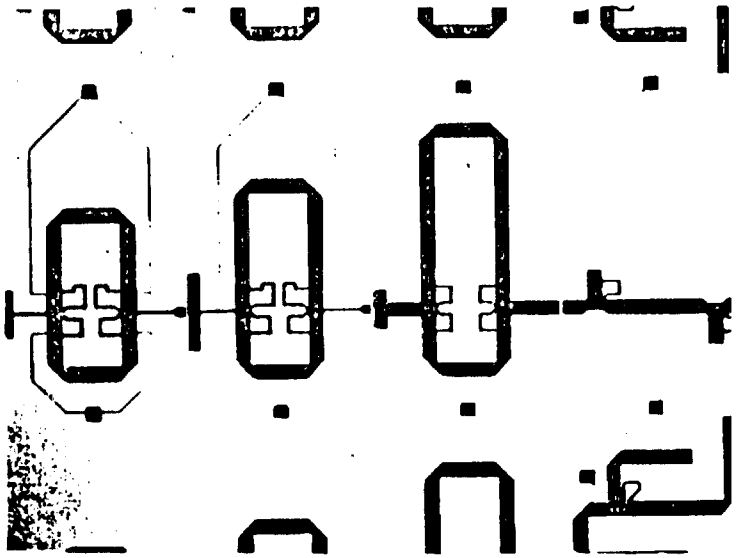
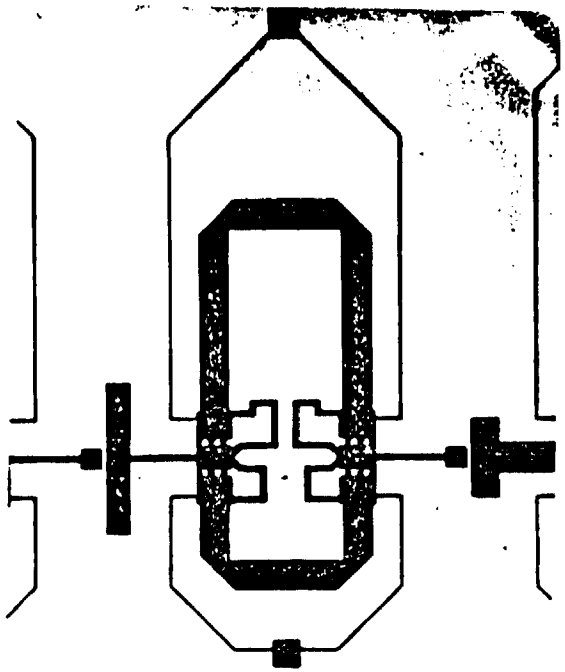


Figure 2-15 Insertion phase results for 180° phase shifter (with shunt FETs).



(a)



(b)

Figure 2-17 (a) Four bit phase shifter.

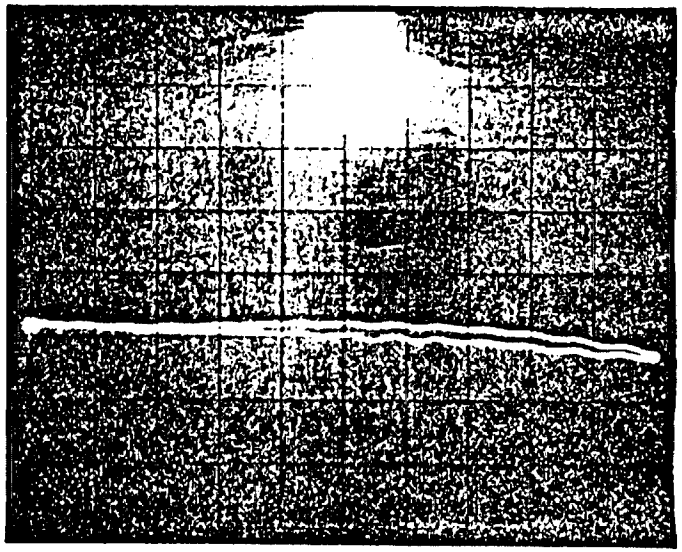


FIGURE 2-16 (b)

Figure 2-16 (b) Measured insertion loss for the two states of the 180° phase shifter.

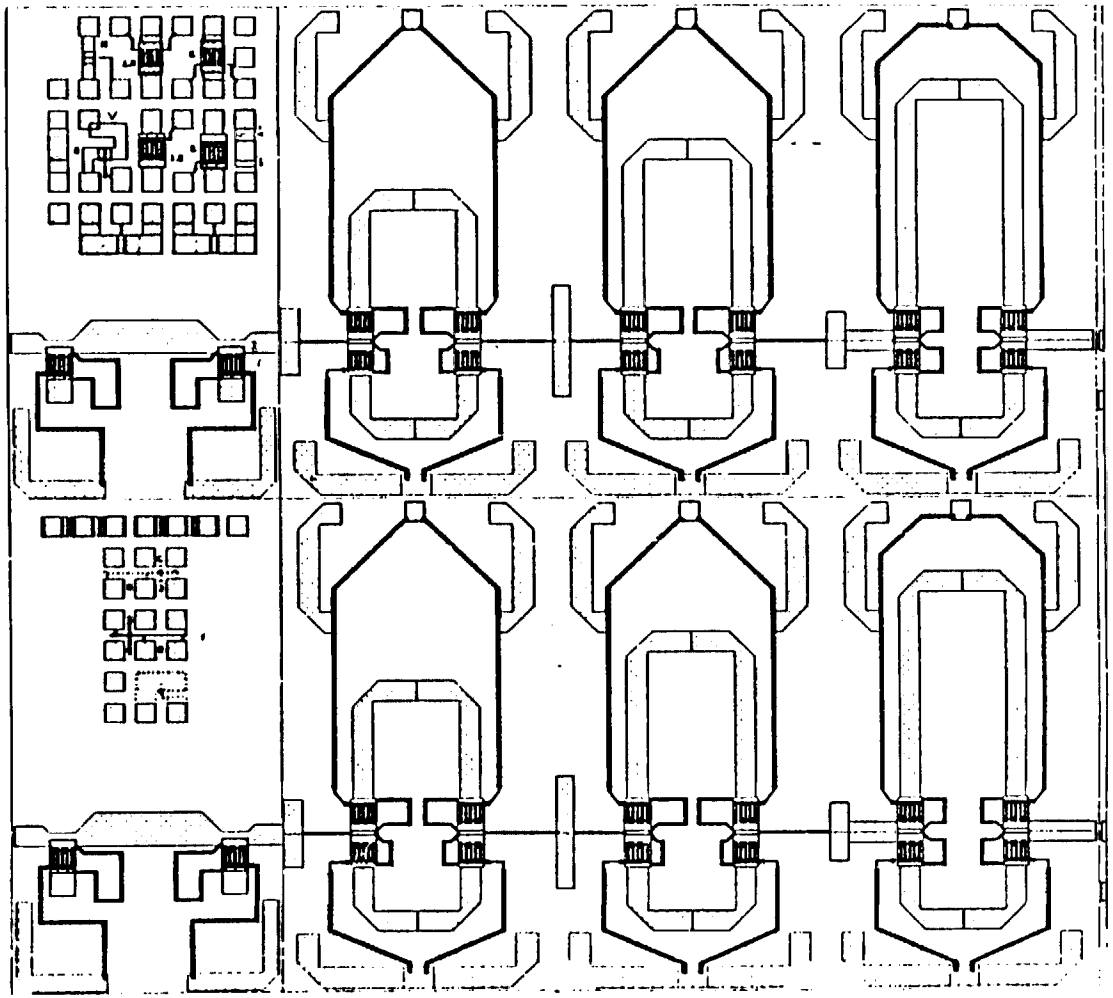


Figure 2-18 (a) Final 5-bit phase shifter layout with the 5th bit incorporated in the 22.5° loaded line bit. Bias circuitry is included on-chip.

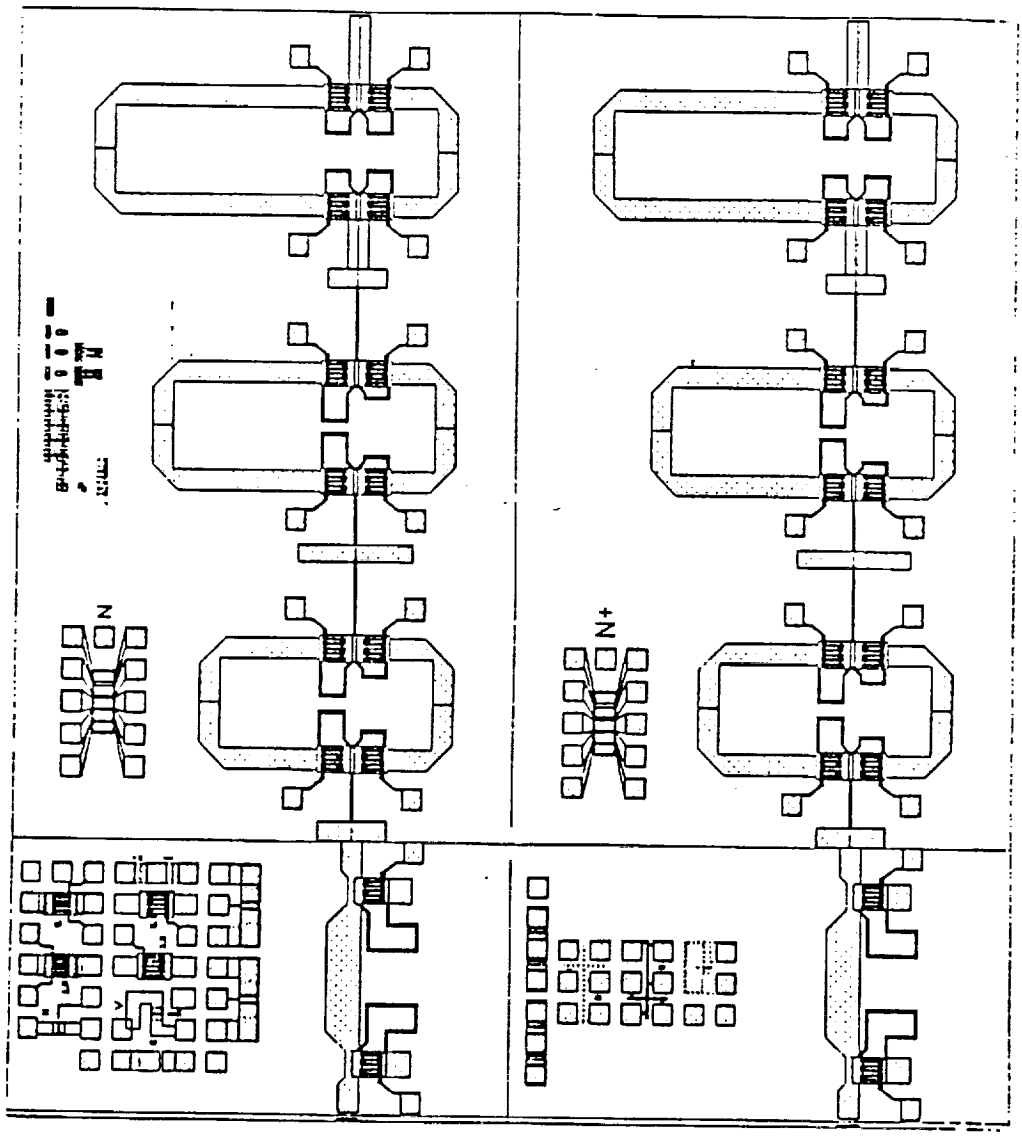
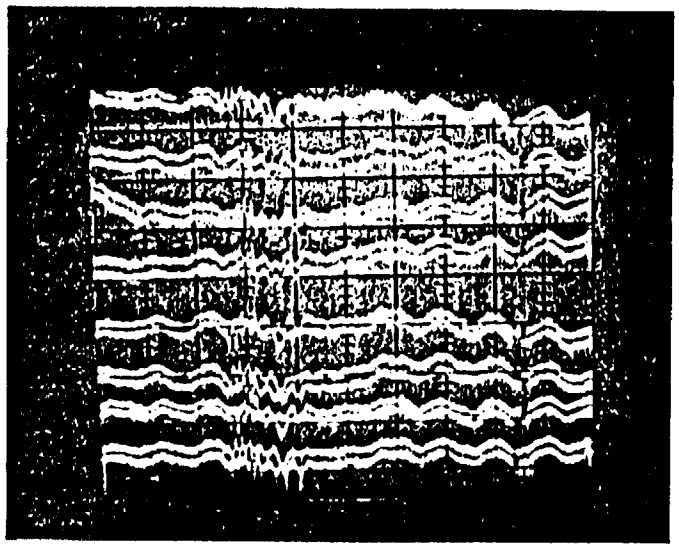


FIGURE 2-18 (b) Final 5-bit phase shifter layout (backup) with no on-chip bias circuit.

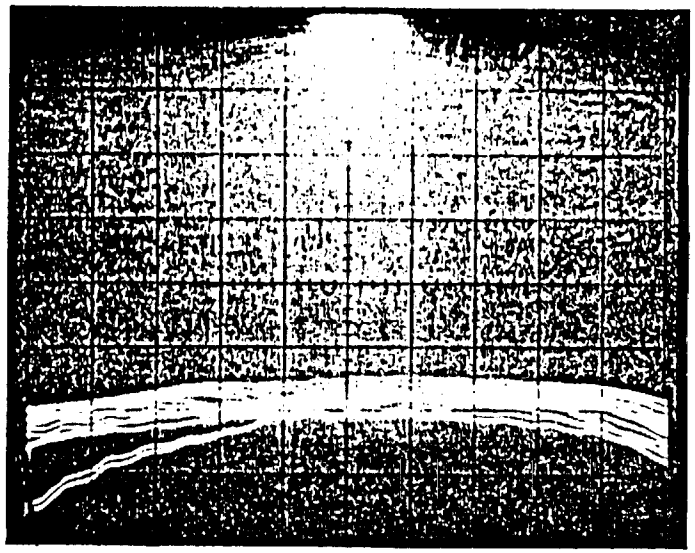


27.5 — 30 GHz

VERT: 45°/DIV

HORIZ: 250 MHz/DIV

(a) Superimposed Differential Insertion Phase Characteristics



27.5 — 32.5 GHz

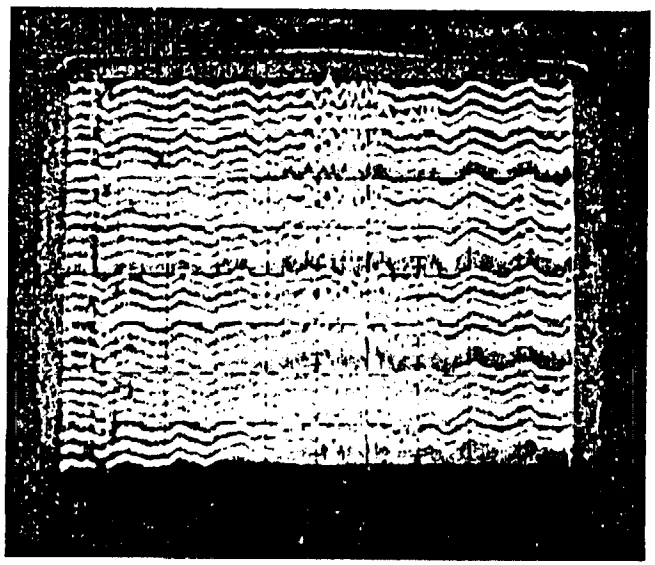
VERT: 4 dB/DIV

HORIZ: 500 MHz/DIV

REF: CENTER LINE

(b) Superimposed Insertion Loss Characteristics

FIGURE 2-18 (c) Superimposed phase and insertion loss characteristics for sixteen states of the design in Figure 2-18 (a).

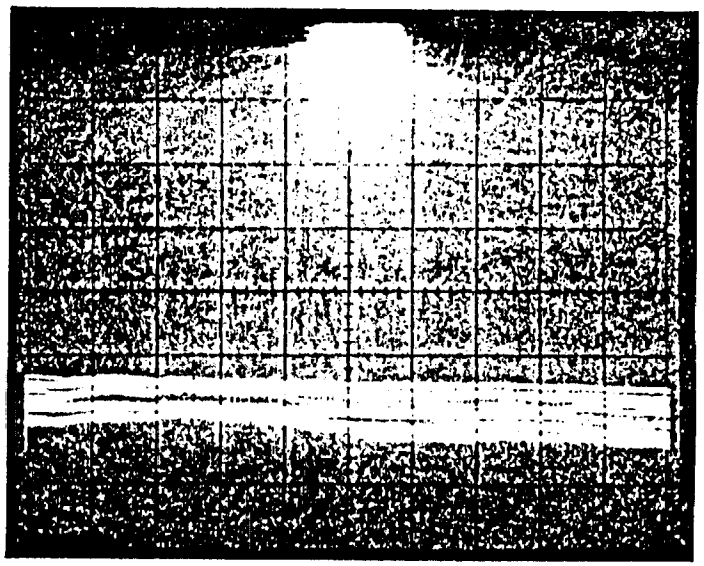


27.5 – 30 GHz

VERT: 45°/DIV

HORIZ: 250 MHz/DIV

(a) Superimposed Differential Insertion Phase Characteristics



27.5 – 30 GHz

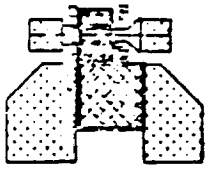
VERT: 5 dB/DIV

HORIZ: 250 MHz/DIV

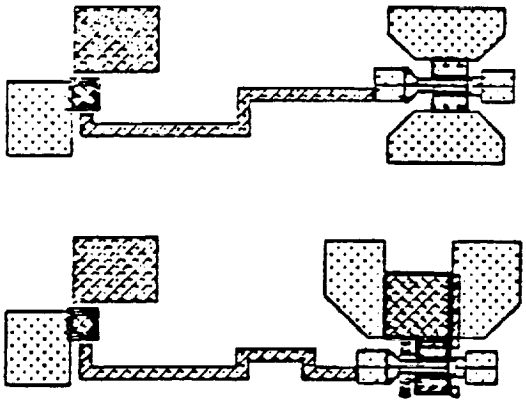
REF: CENTER LINE

(b) Superimposed Insertion Loss Characteristics

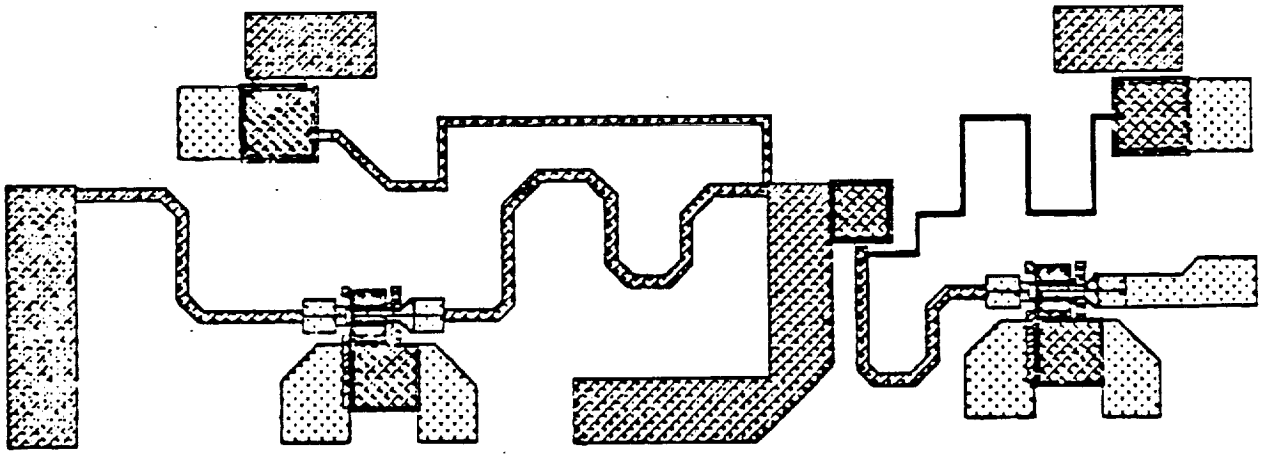
FIGURE 2-15 (d) Superimposed phase and insertion loss characteristics for 32 states of the design in Figure 2-18 (b).



A) DISCRETE DUAL GATE FET

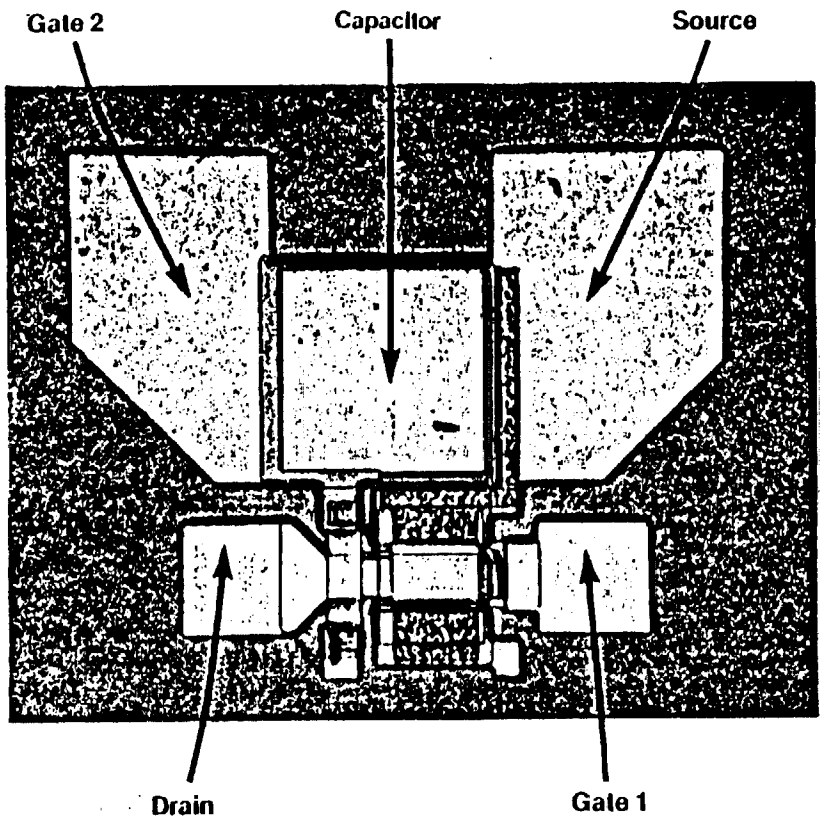


B) SINGLE AND DUAL GATE FETS WITH INPUT MATCHING



C) 2-STAGE DUAL GATE AMPLIFIER

Figure 2-19 (a) Discrete dual gate FET.
(b) Single and dual gate FETs with input matching.
(c) 2-Stage dual gate amplifier.



Dual Gate FET

DC-IV

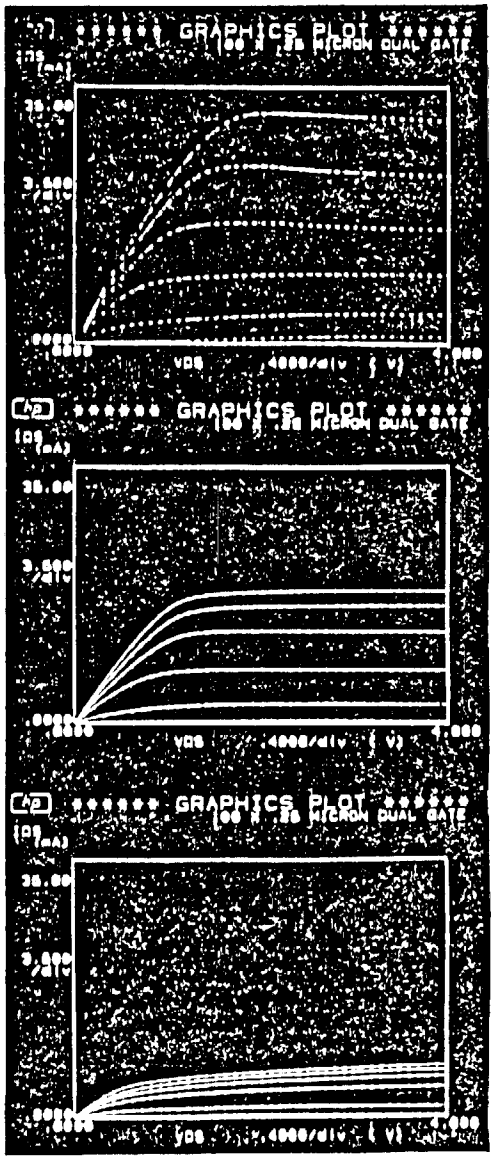
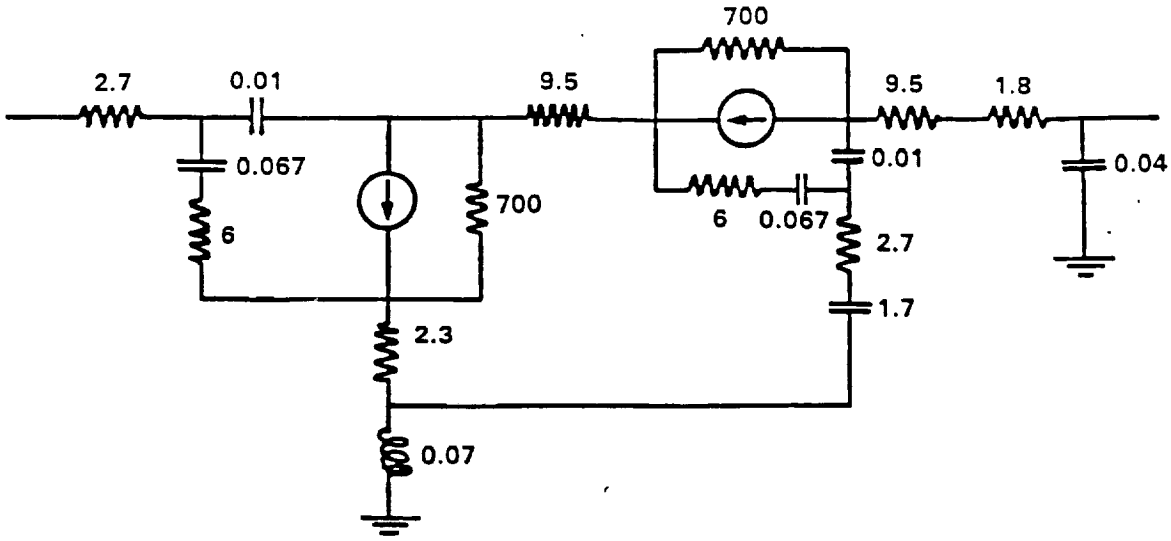
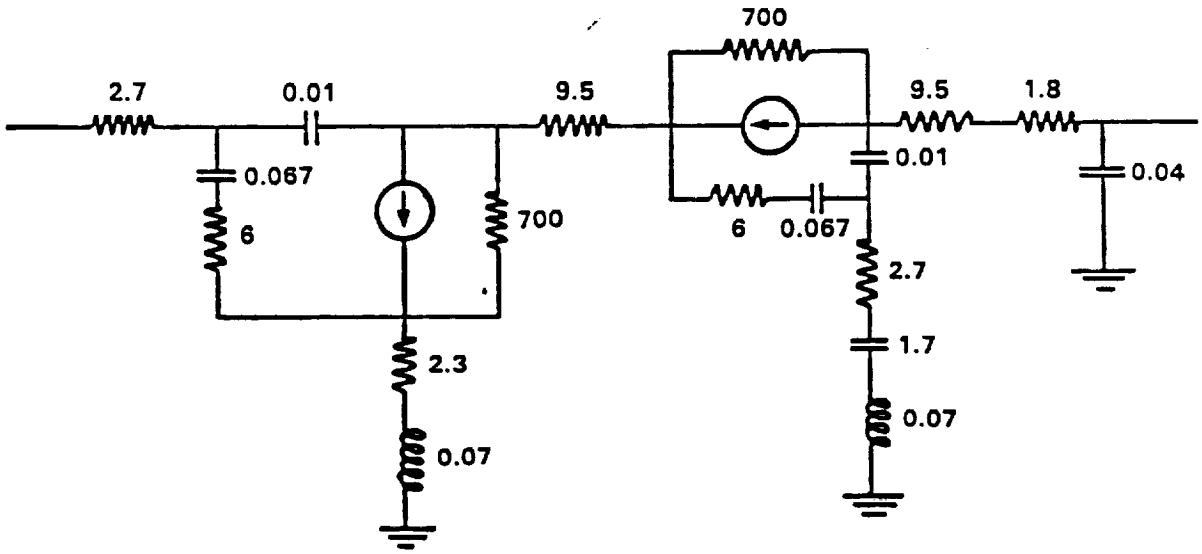


Figure 2-20 A fabricated dual gate FET (0.25 x 100 μm^2) with the dc characteristics.



(a) OLD DUAL GATE FET



(b) MODIFIED DUAL GATE FET

Figure 2-21 (a) Schematic for old dual-gate FET layout.
(b) Schematic for new dual gate FET layout.

DGF4A

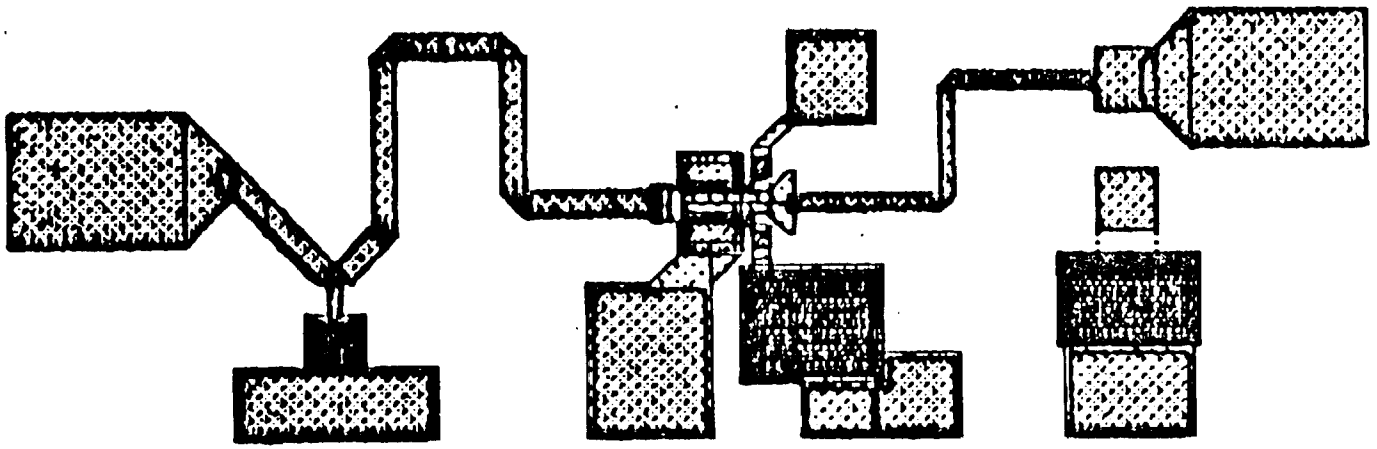


FIGURE 2-22(a)

Magnification — 150X

DGF2A

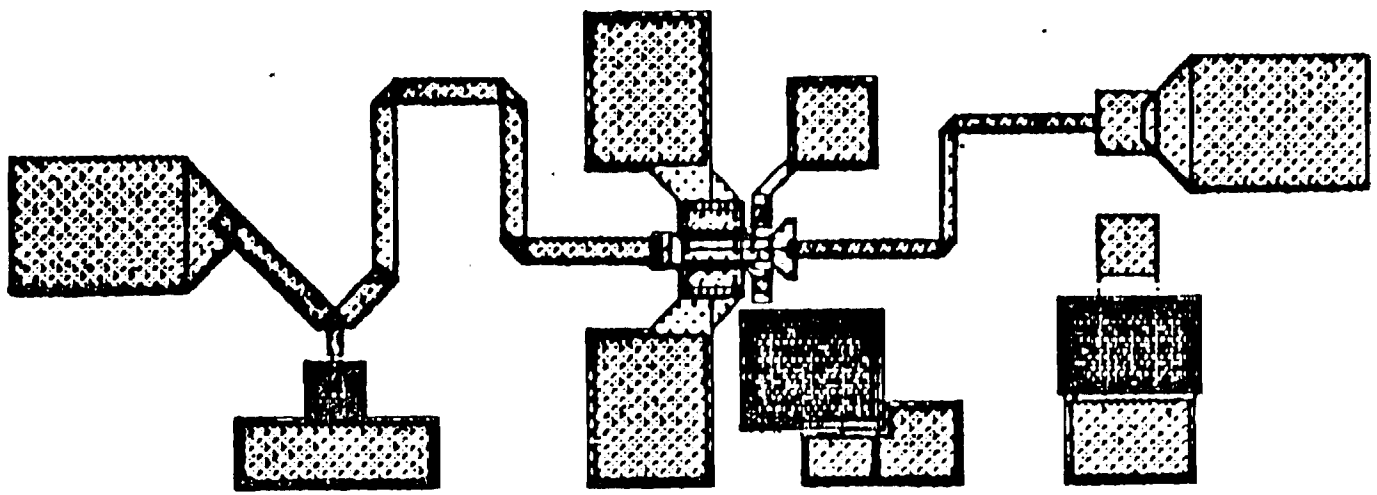


FIGURE 2-22 (b)

Magnification — 150X

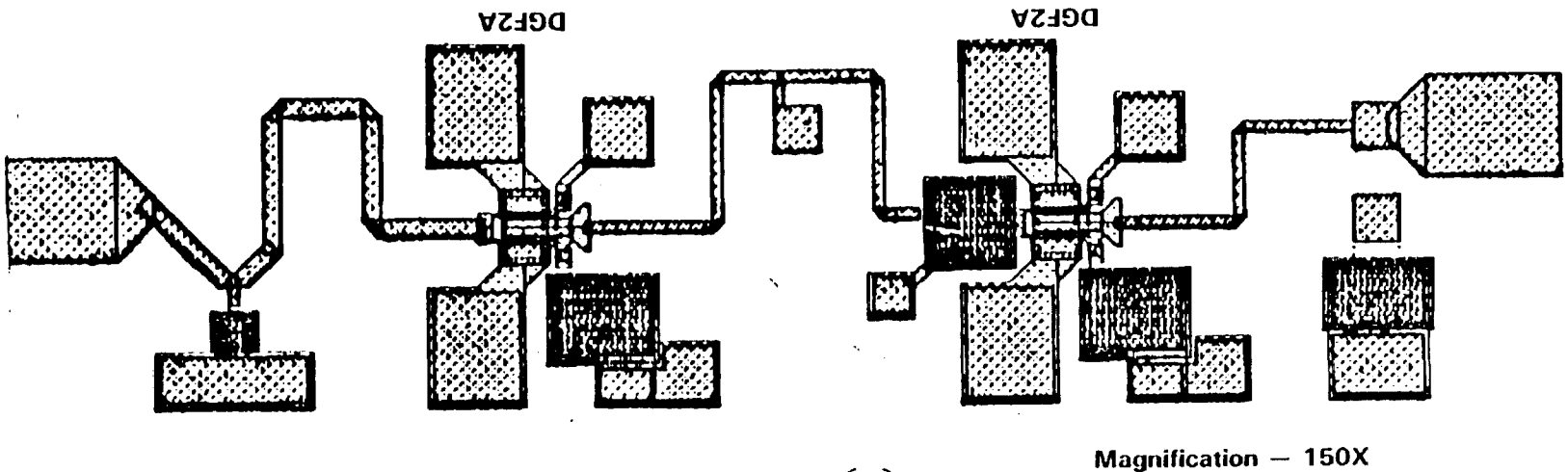


FIGURE 2.22 (c)

Figure 2-22 (a) Layout of single stage dual gate amplifier with single source ground for dual gate FET.

(b) Layout of single stage dual gate amplifier with double source ground for dual gate FET.

(c) Layout of modified two-stage dual gate amplifier.

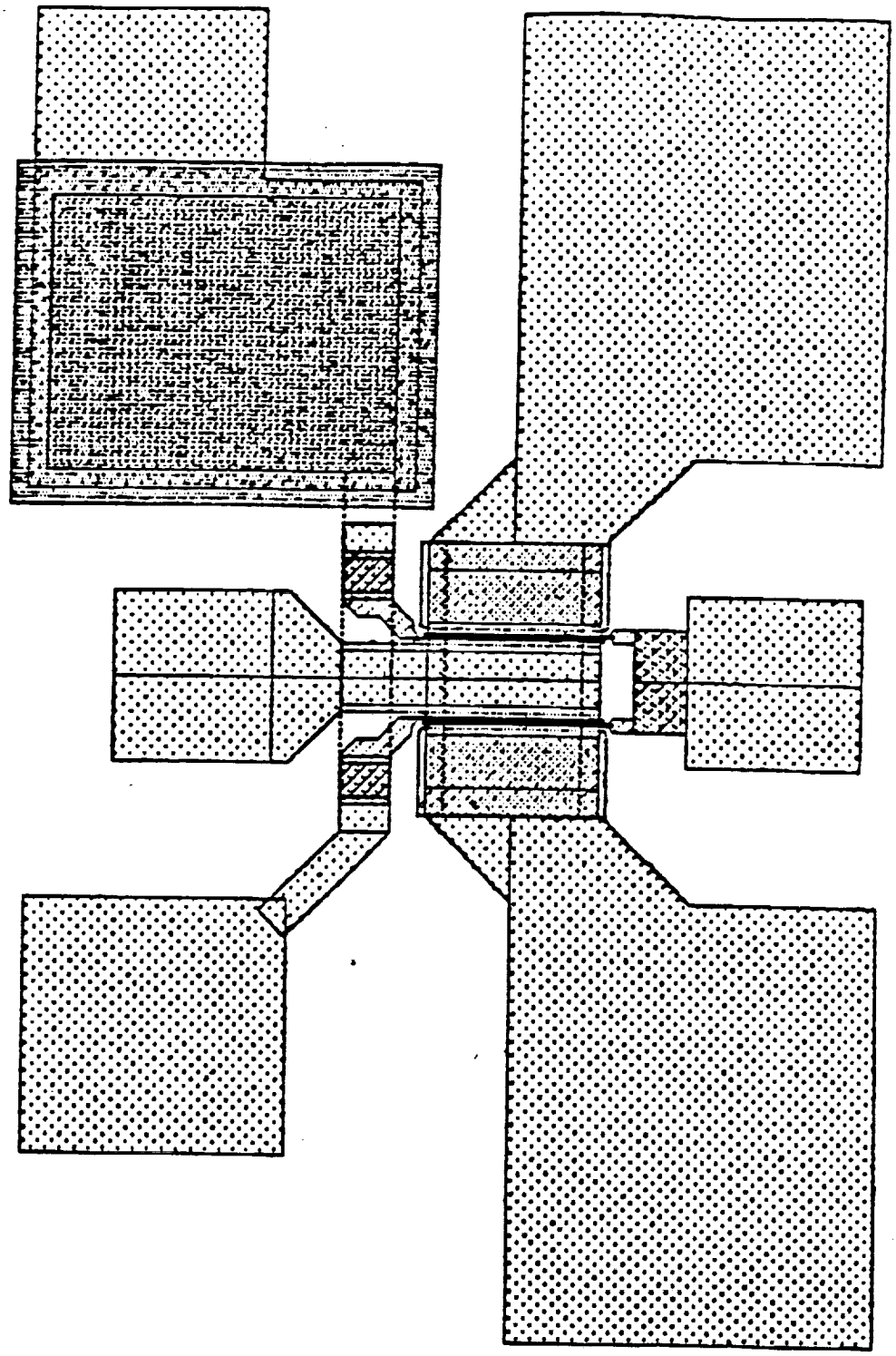


Figure 2-23 Layout of a dual gate FET with two source grounding.

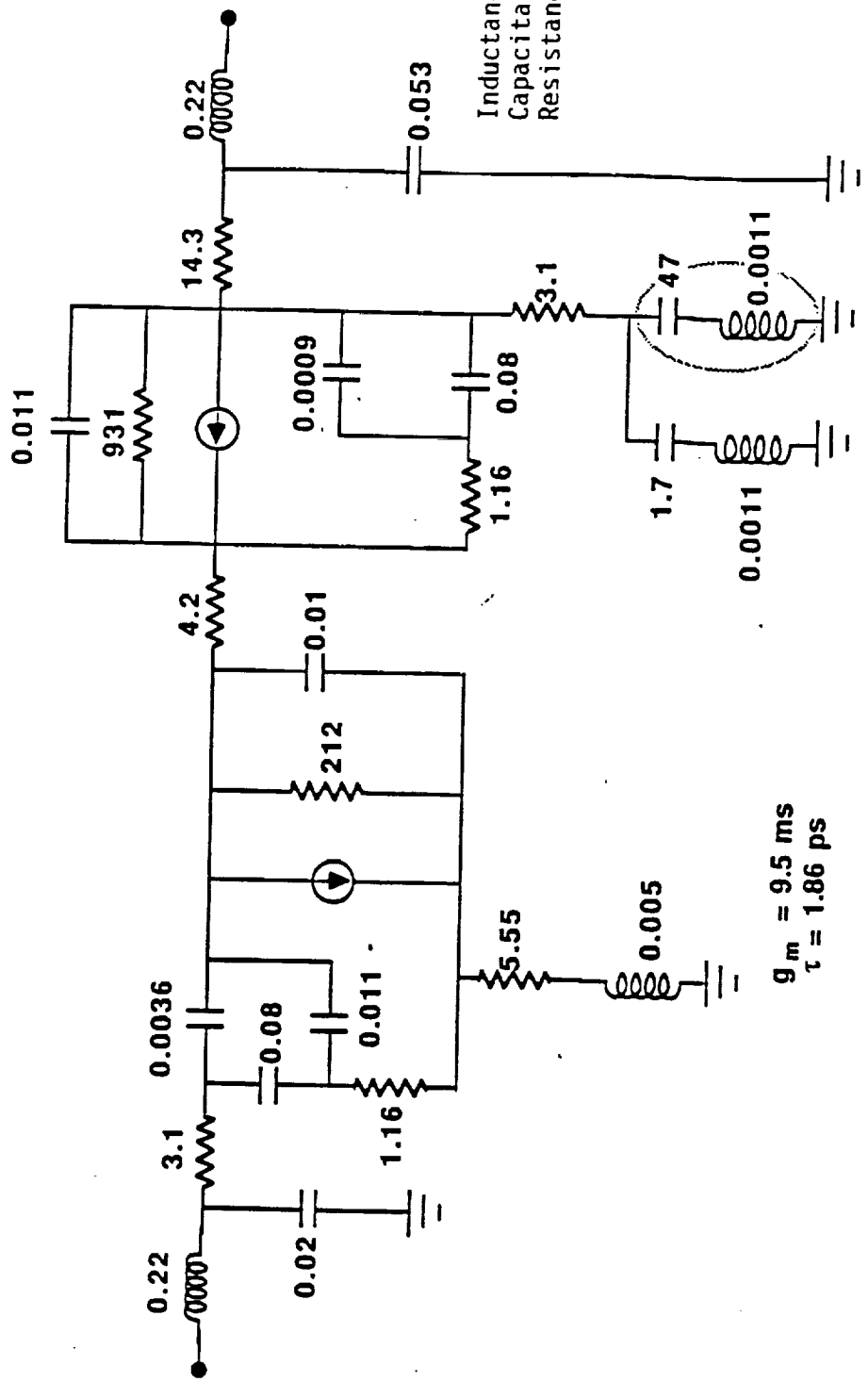


Figure 2-24 Equivalent circuit parameters of the dual gate FET shown in Figure 2-23.

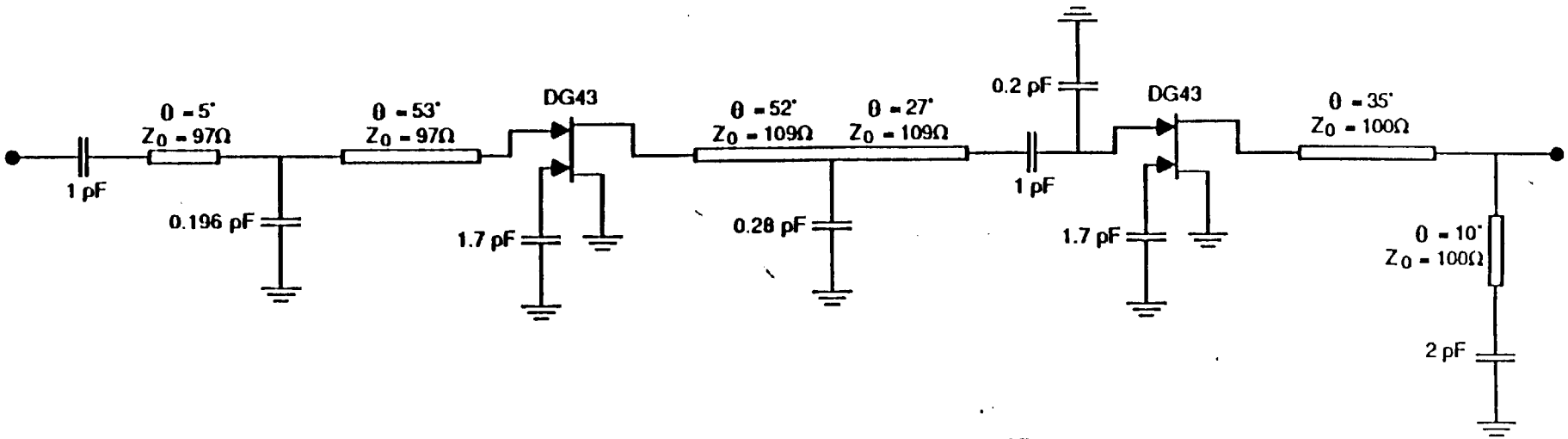


Figure 2-25 Schematic for two-stage dual gate amplifier.

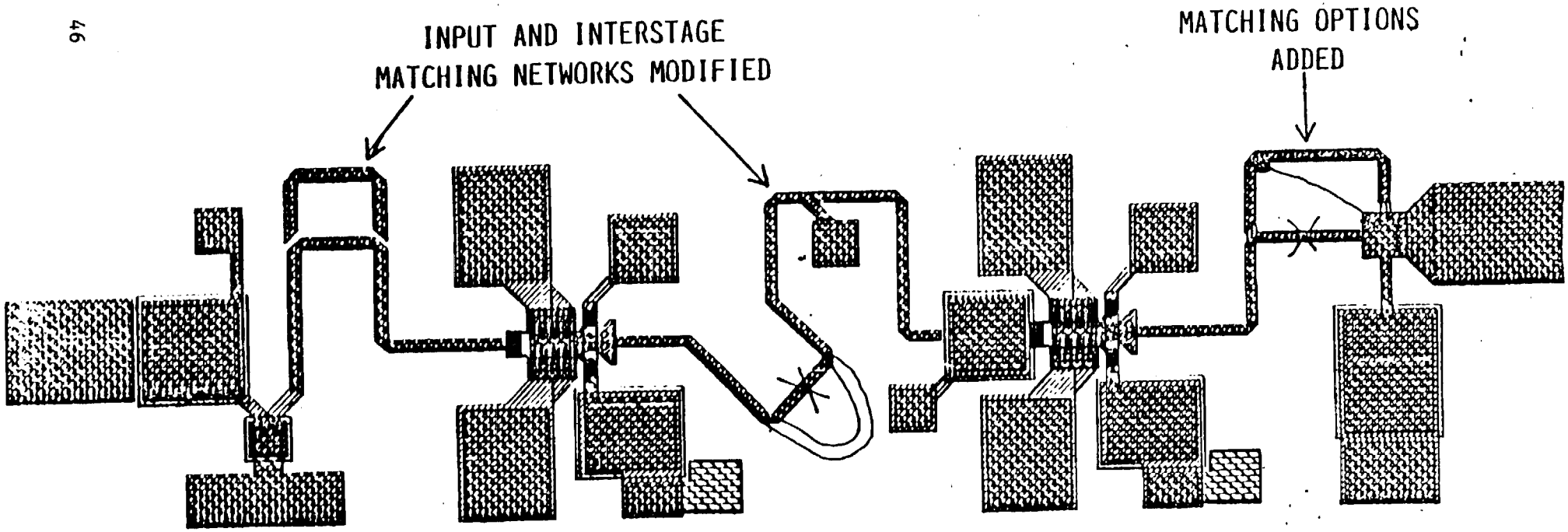


Figure 2-26 On-chip RF tuning of the two-stage dual gate amplifier.

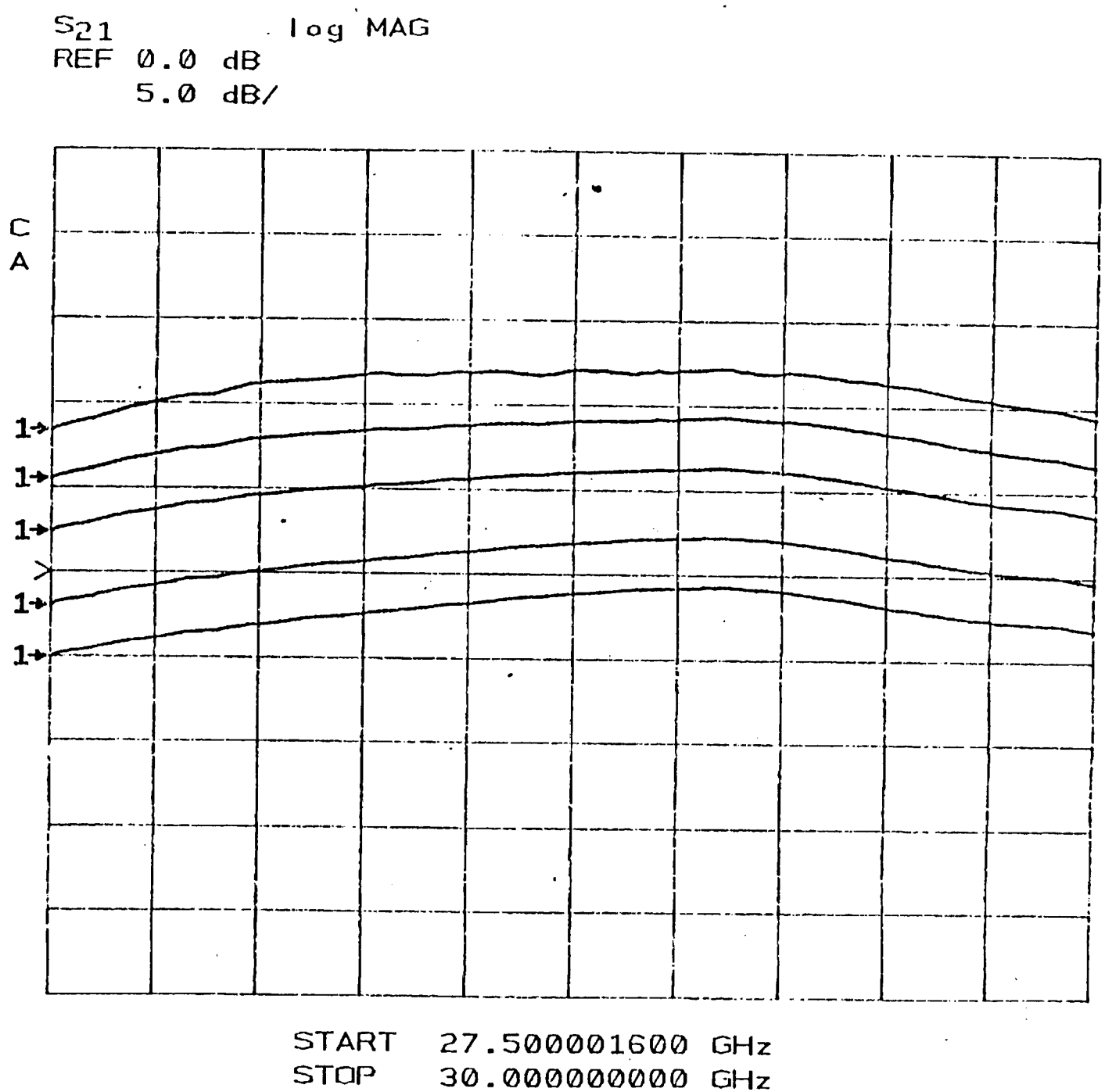


Figure 2-27 (a) Dual gate two-stage amplifier response with on-chip tuning for the gain variation.

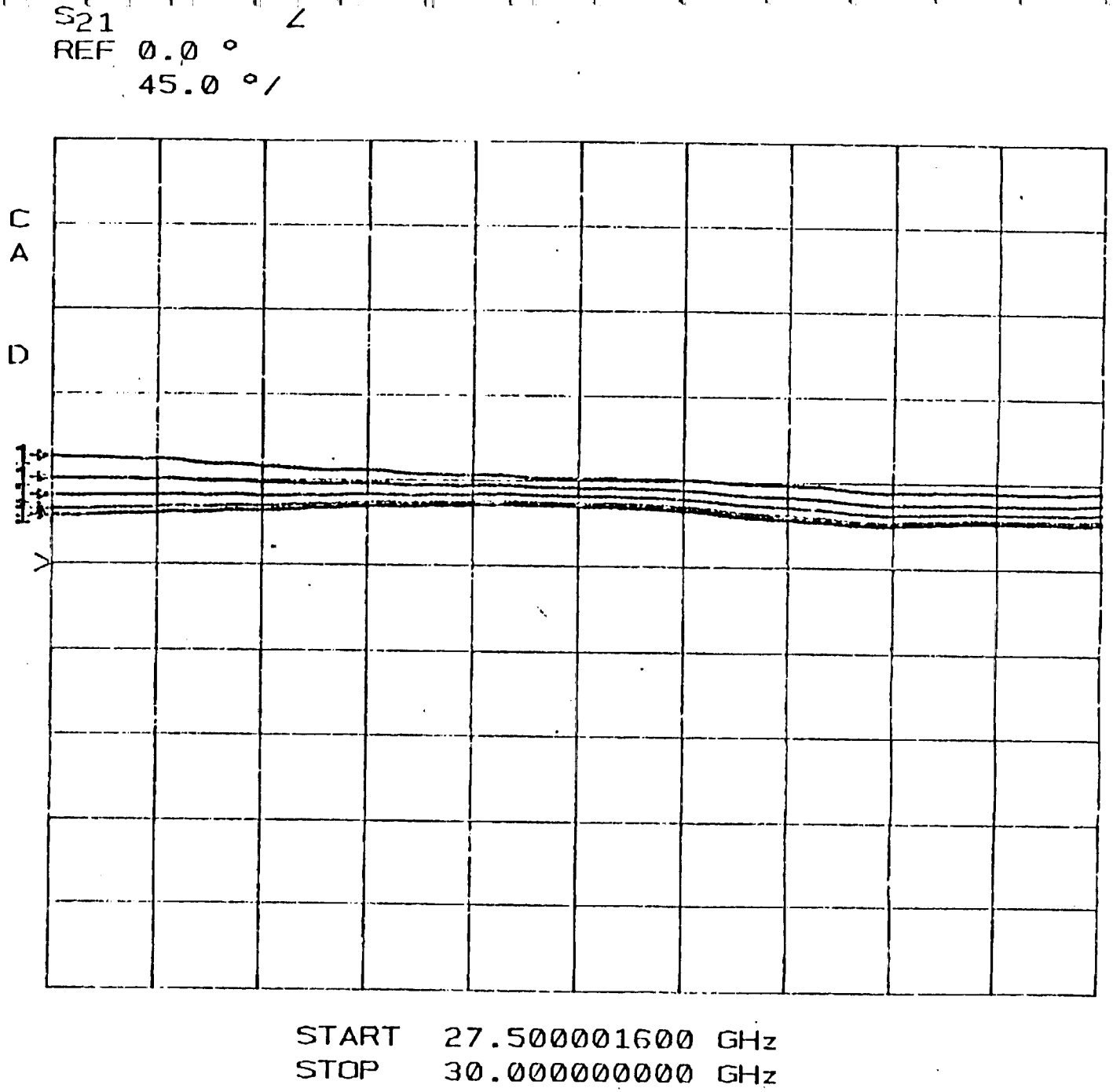


FIGURE 2.27 (b) The phase variation envelope with the gain variation.

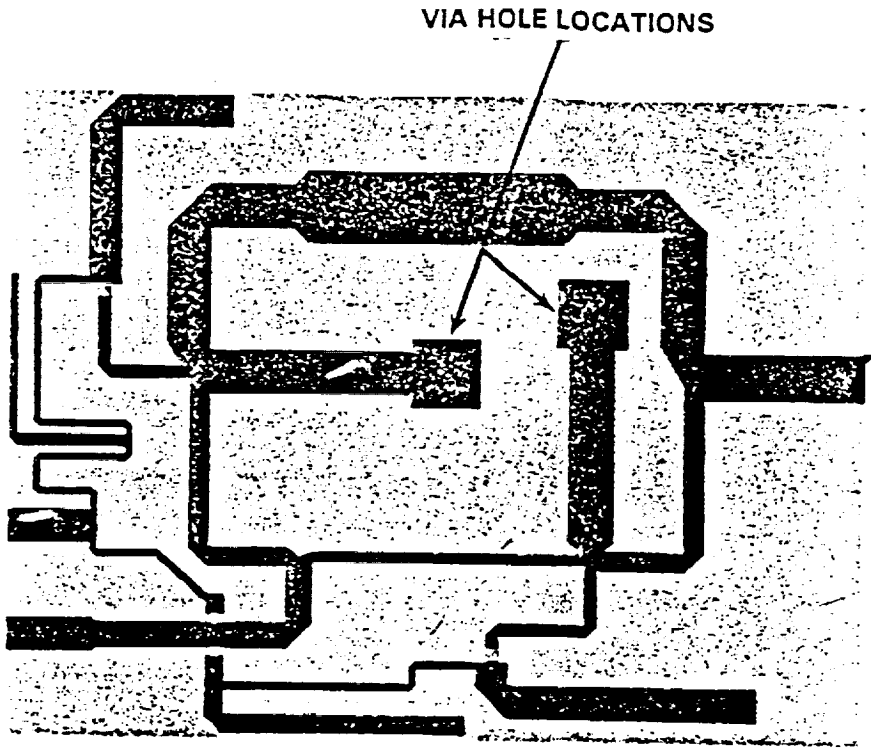


Figure 2-28 Fabricated chip of RF/IF mixer submodule using Schottky diodes and modified rat race hybrid (3.1 x 2.2 x 0.15 mm^3).

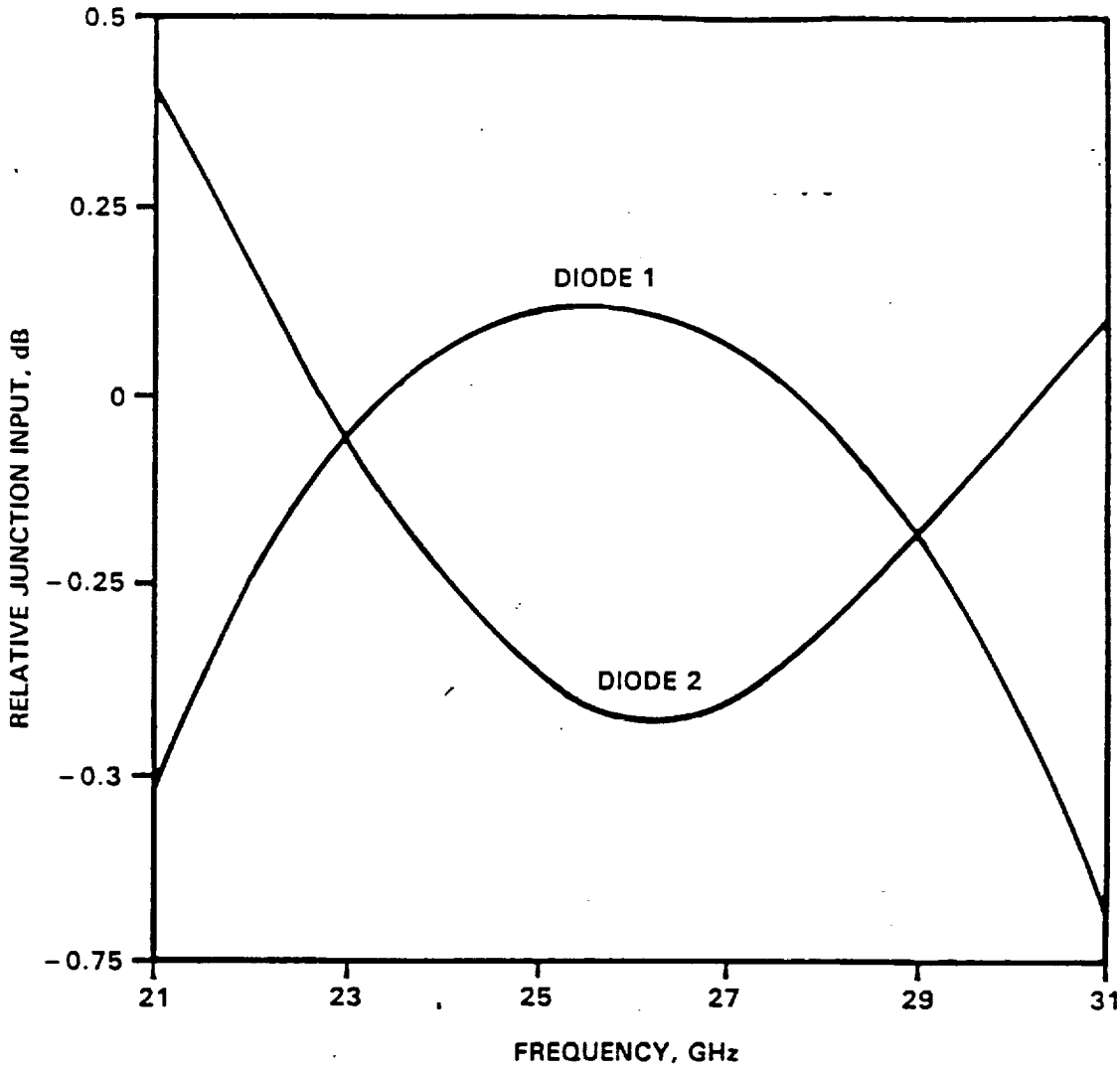


Figure 2-29 RF signal and LO magnitude balance at the two diodes (as calculated).

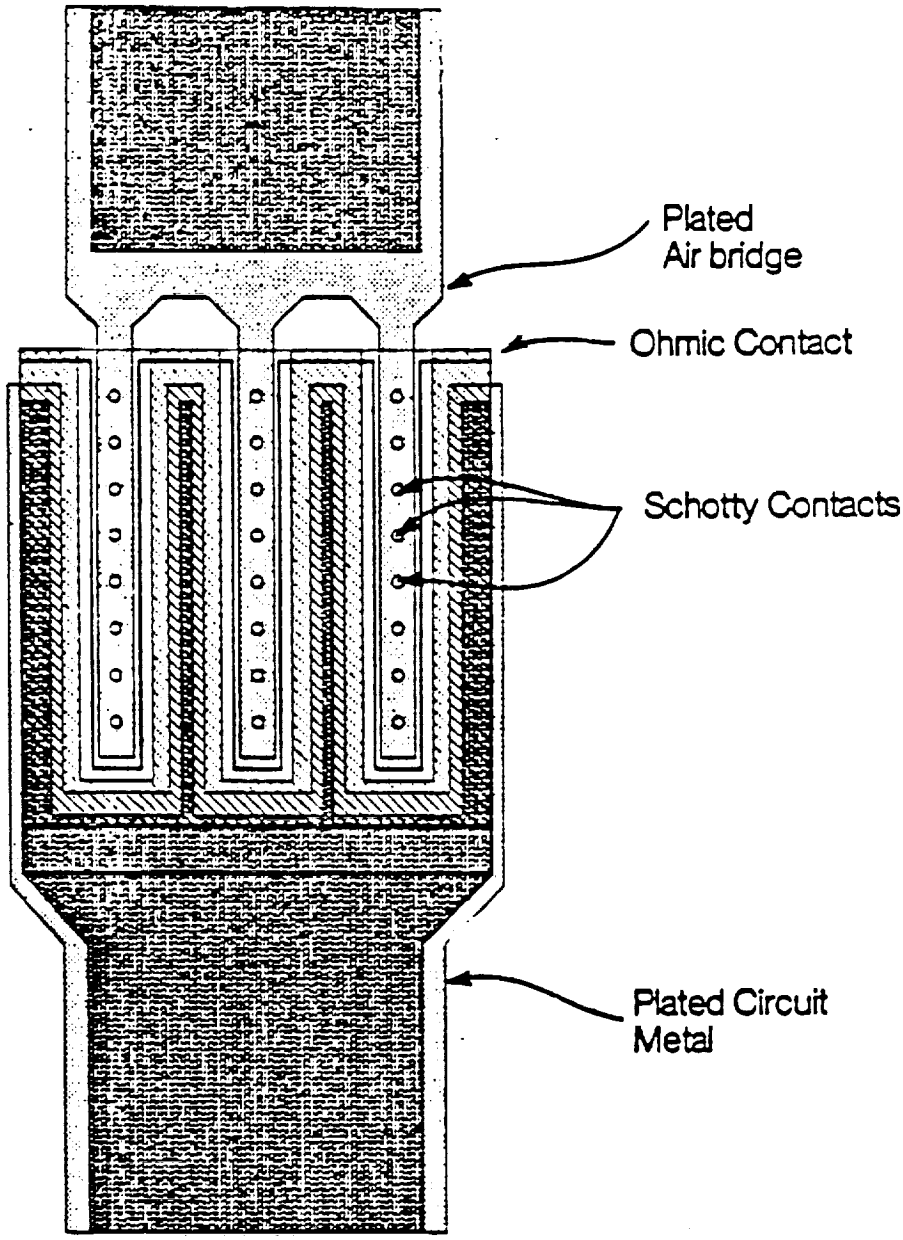


Figure 2-30 CALMA layout of ion implanted mixer diode shown 1 μm Schottky diodes for reducing the spreading resistance.

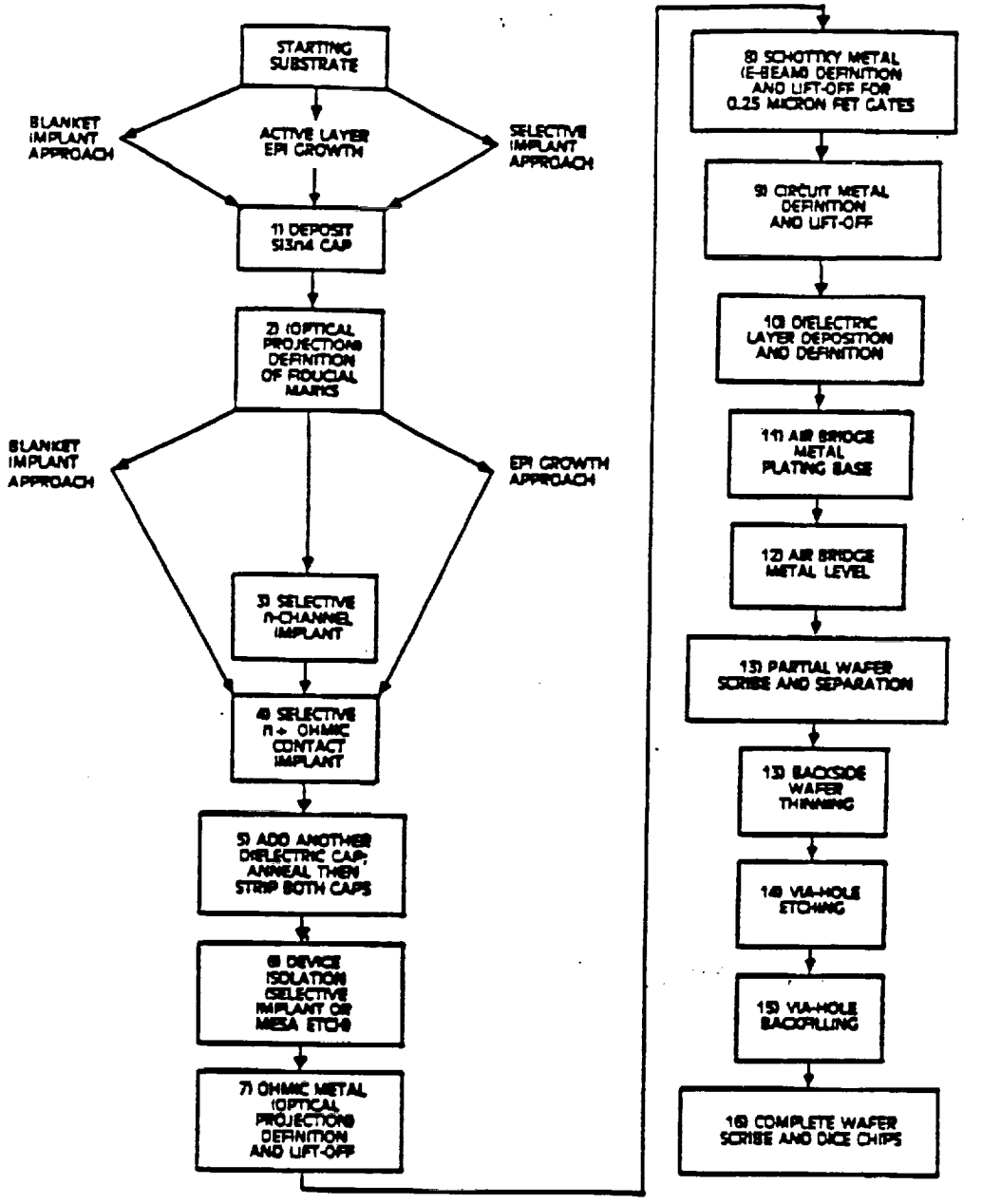


Figure 2-31 Flow chart for e-beam/optical lithography fabrication process to fabricate ion-implanted microdot diodes.

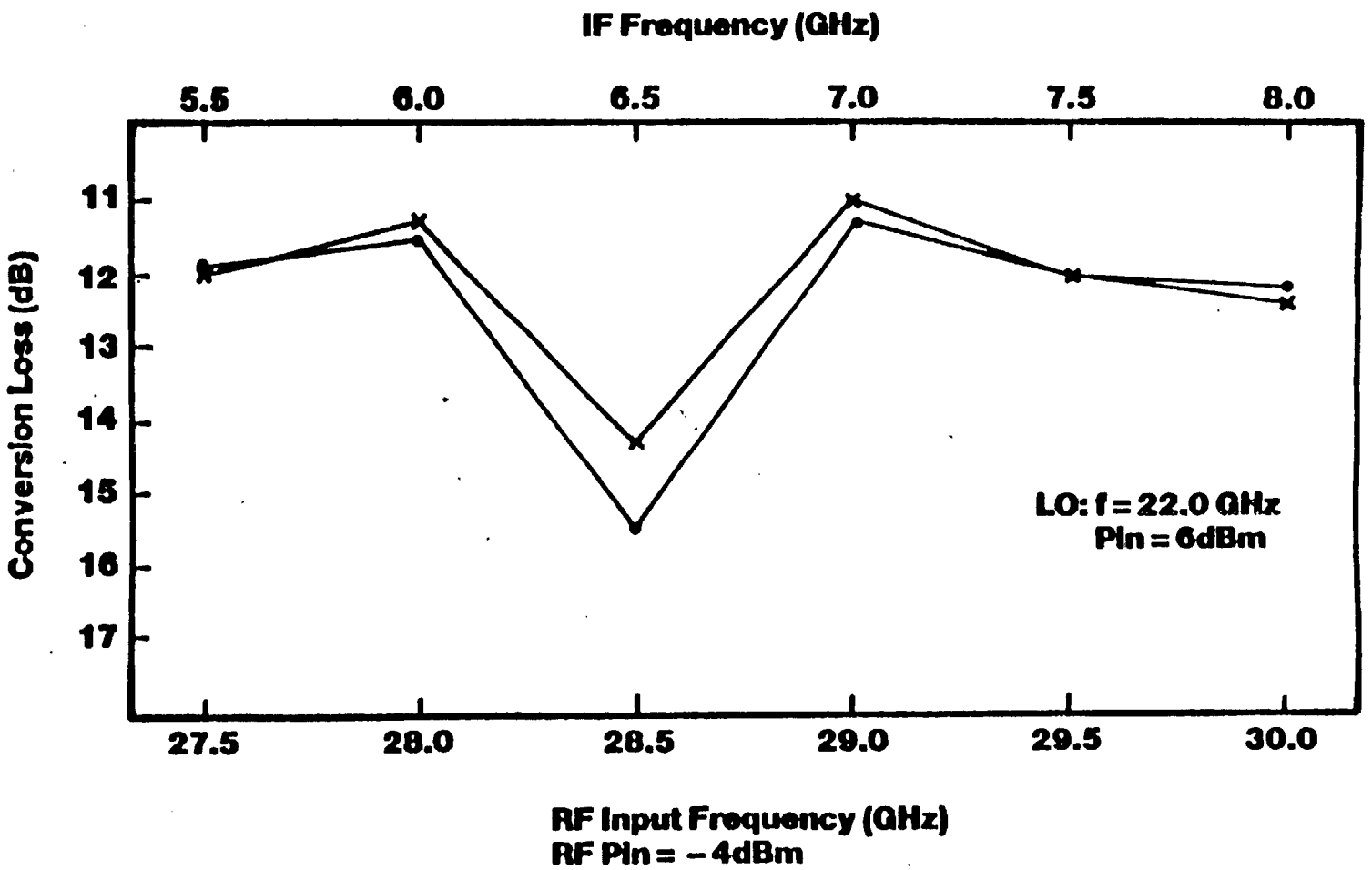


Figure 2-32 Measured insertion loss of two mixer chips from the first iteration.

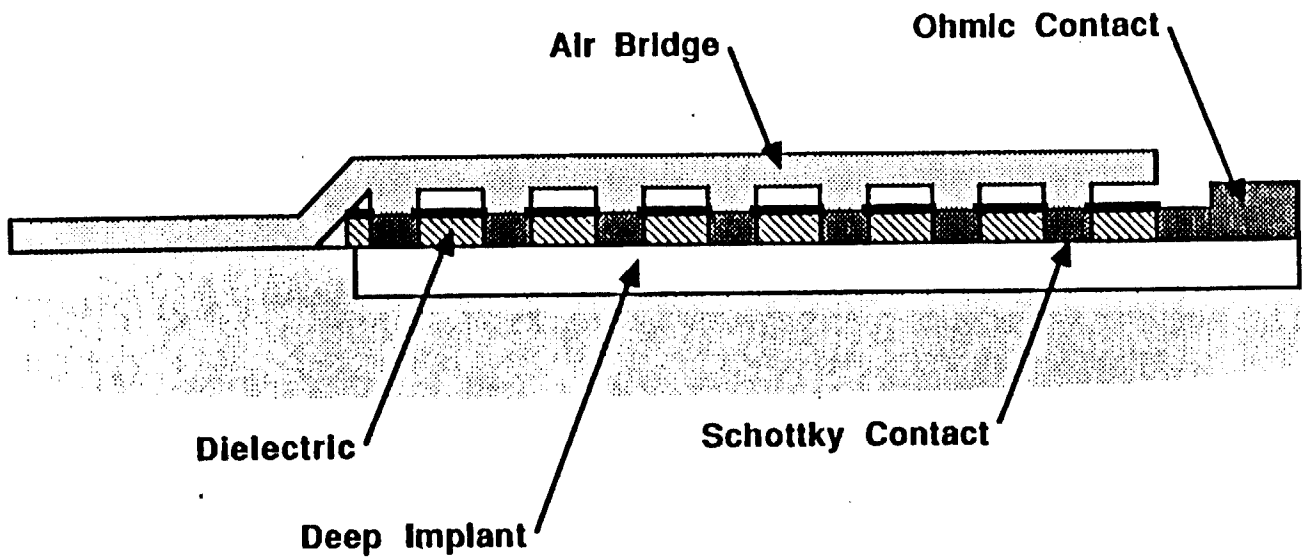


Figure 2-33 Cross section of an ion implanted diode structure.

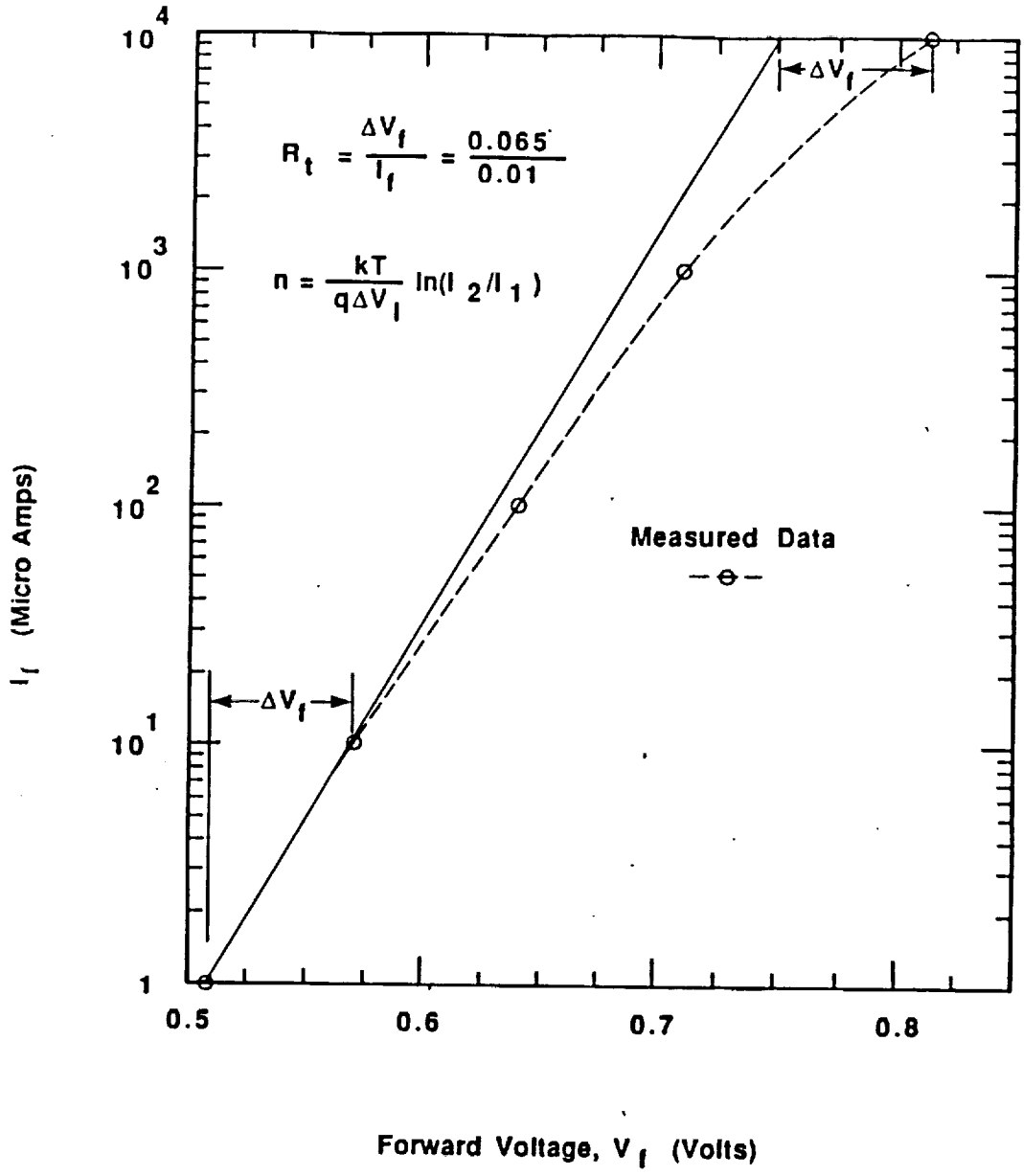


Figure 2-34 Measured I-V characteristics of a diode used in the mixer.

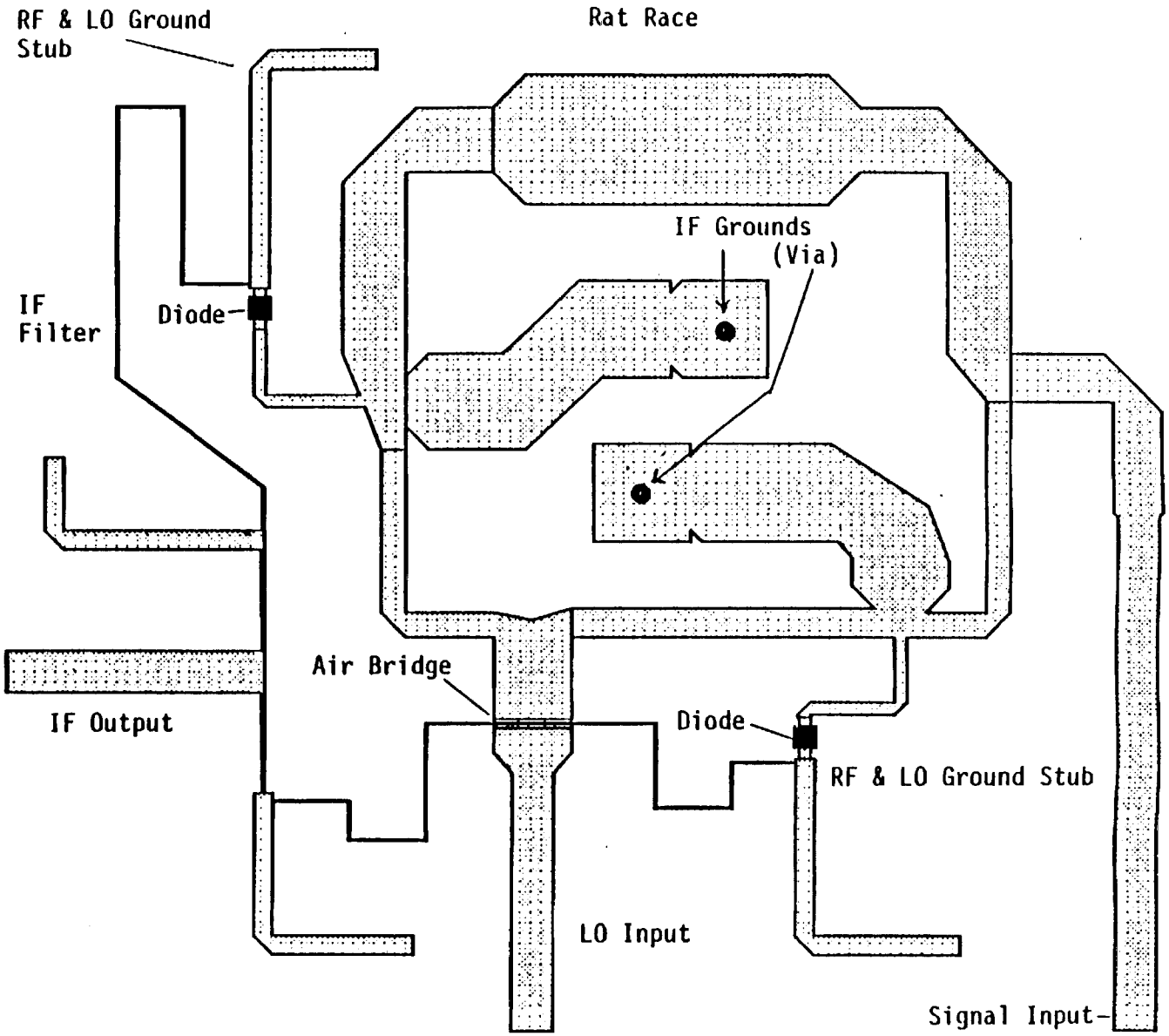


Figure 2-35 The final layout of the RF/IF mixer with IF filter.

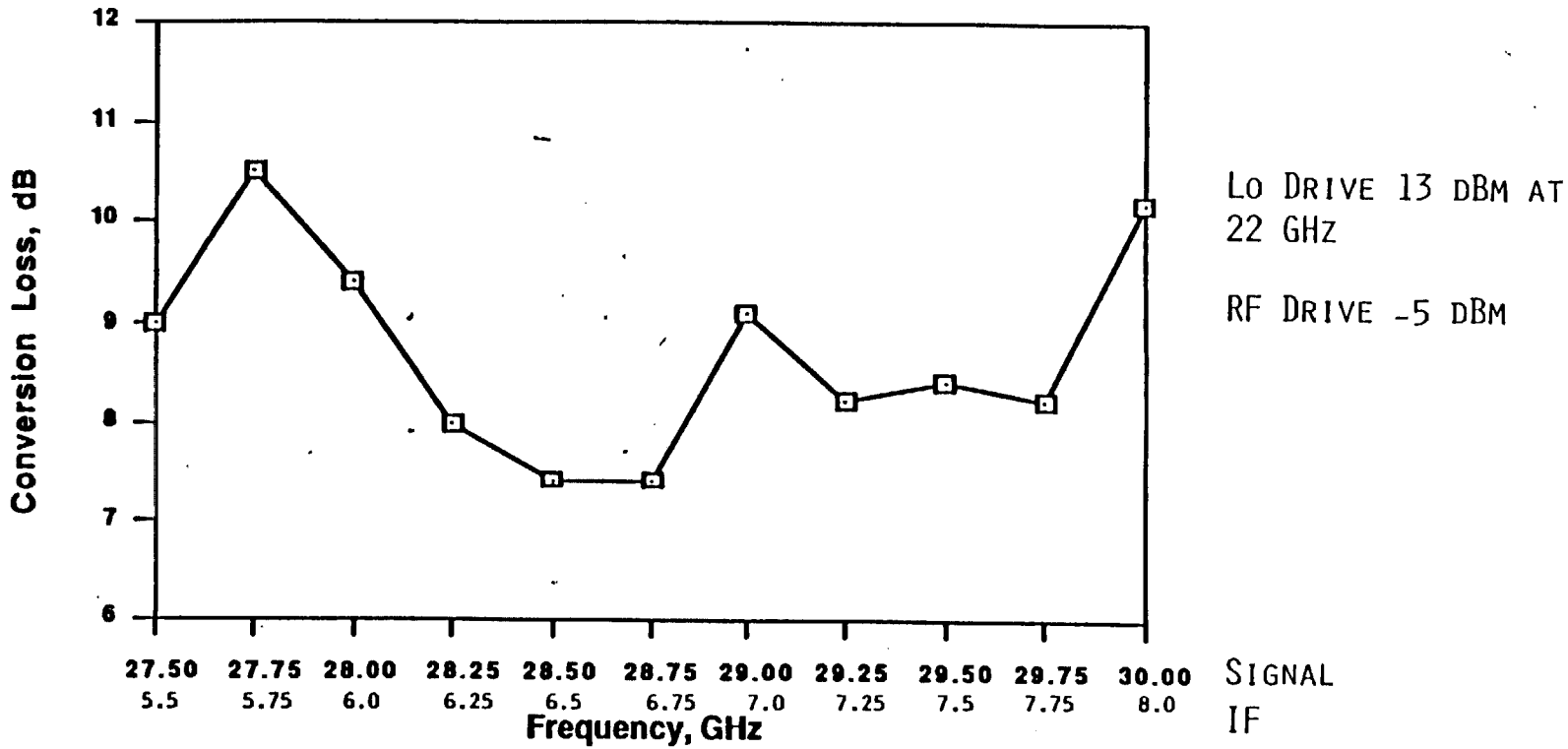


Figure 2-36 The conversion loss performance of the mixer as measured with 13 dBm of local oscillator power.

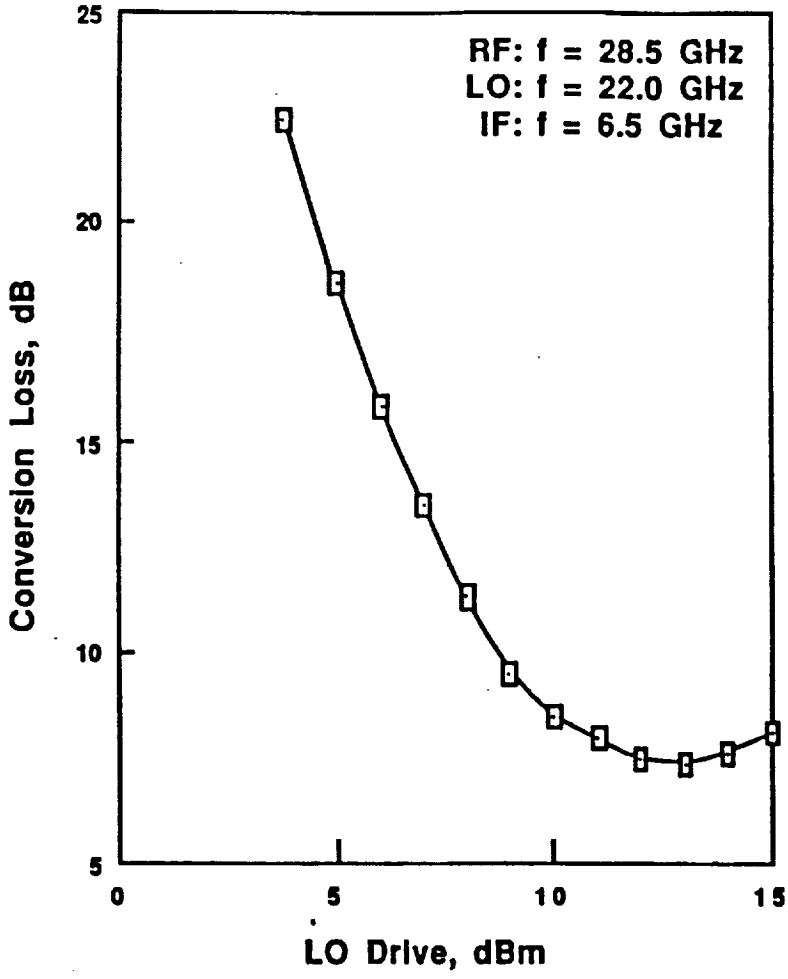


Figure 2-37 Conversion loss vs. LO drive. The best mixer performance occurred at 13 dB of local oscillator power.

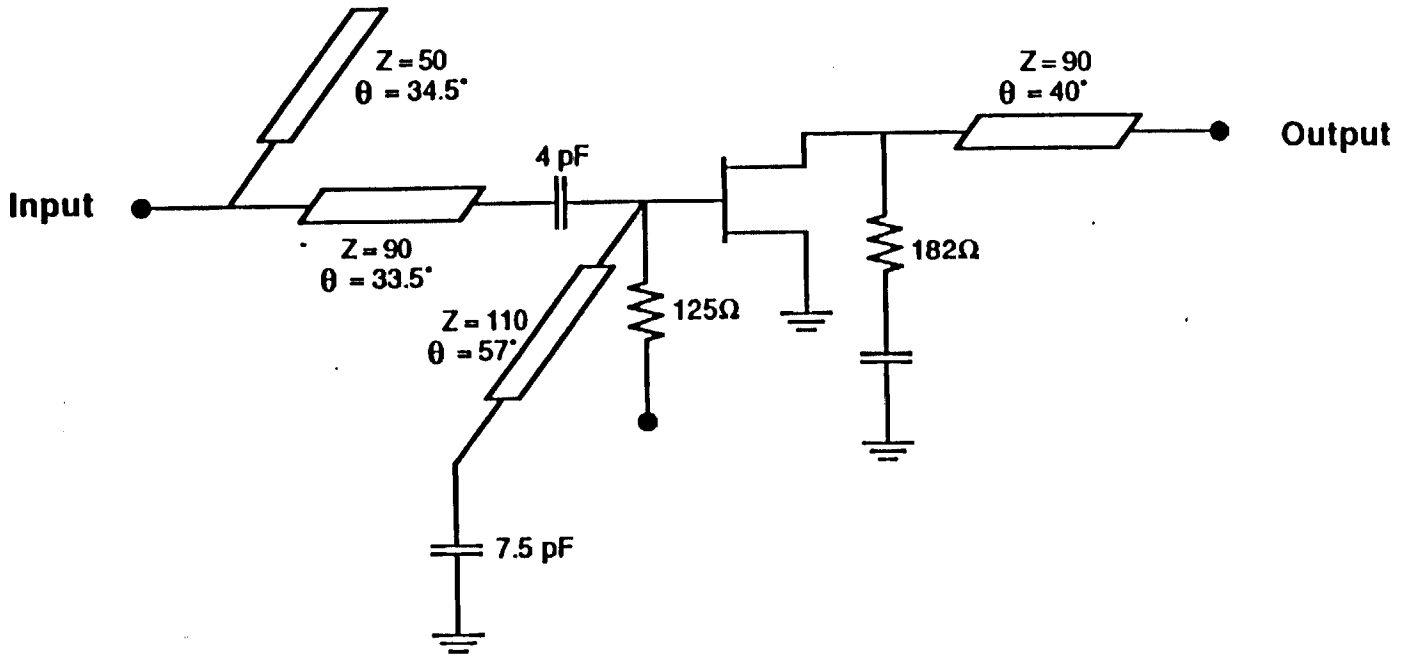


Figure 2-38 The schematic of IF amplifier.

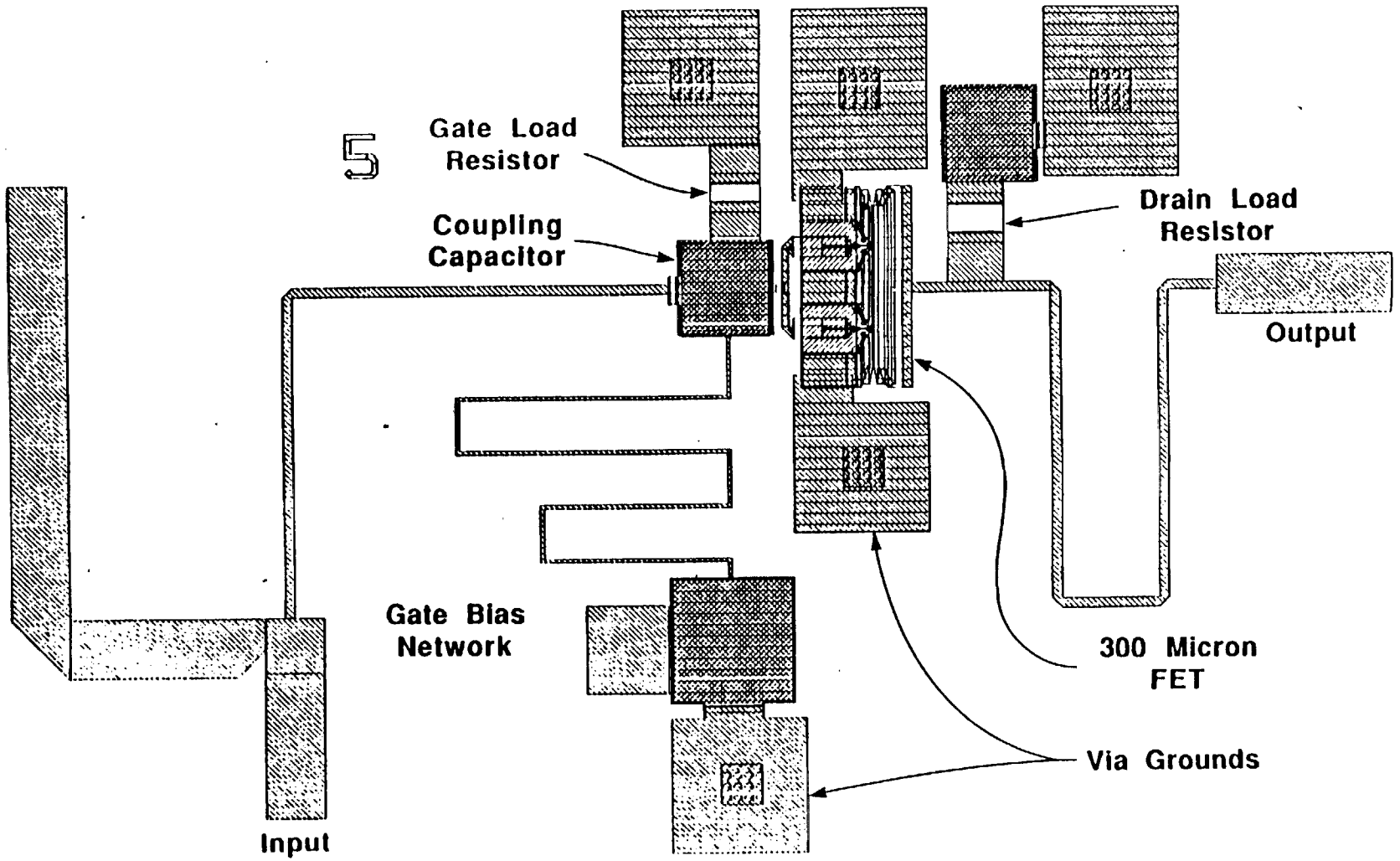


Figure 2-39 The layout of IF amplifier circuit.

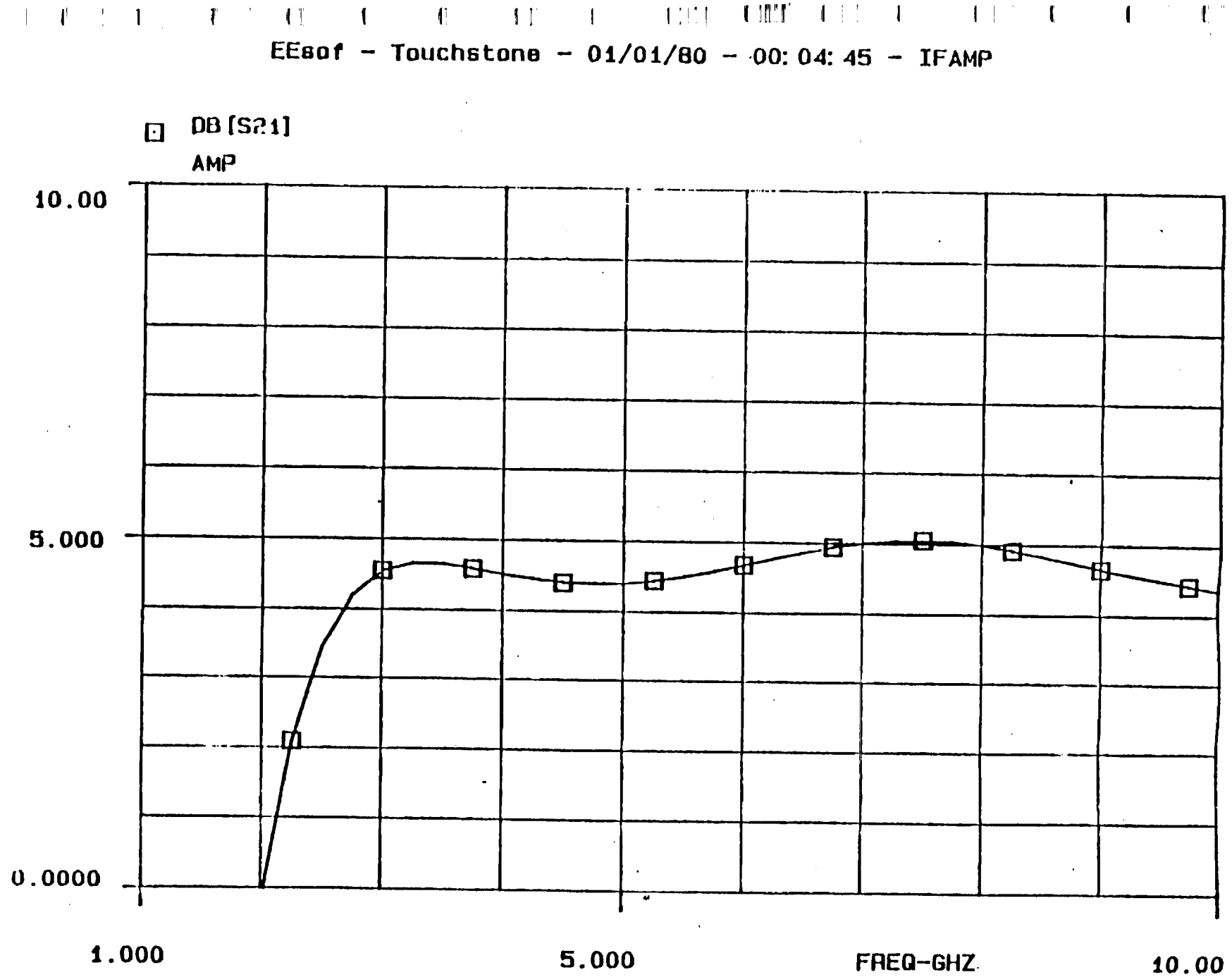
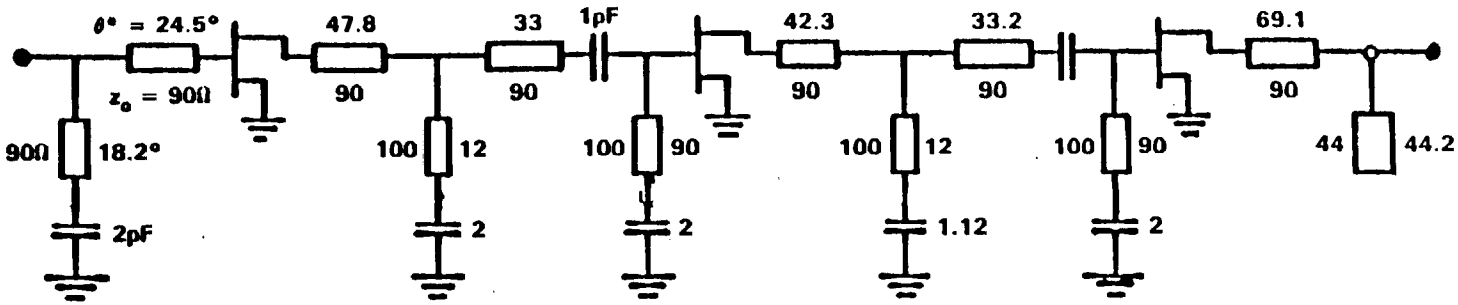


Figure 2-40 Calculated IF amplifier frequency response.



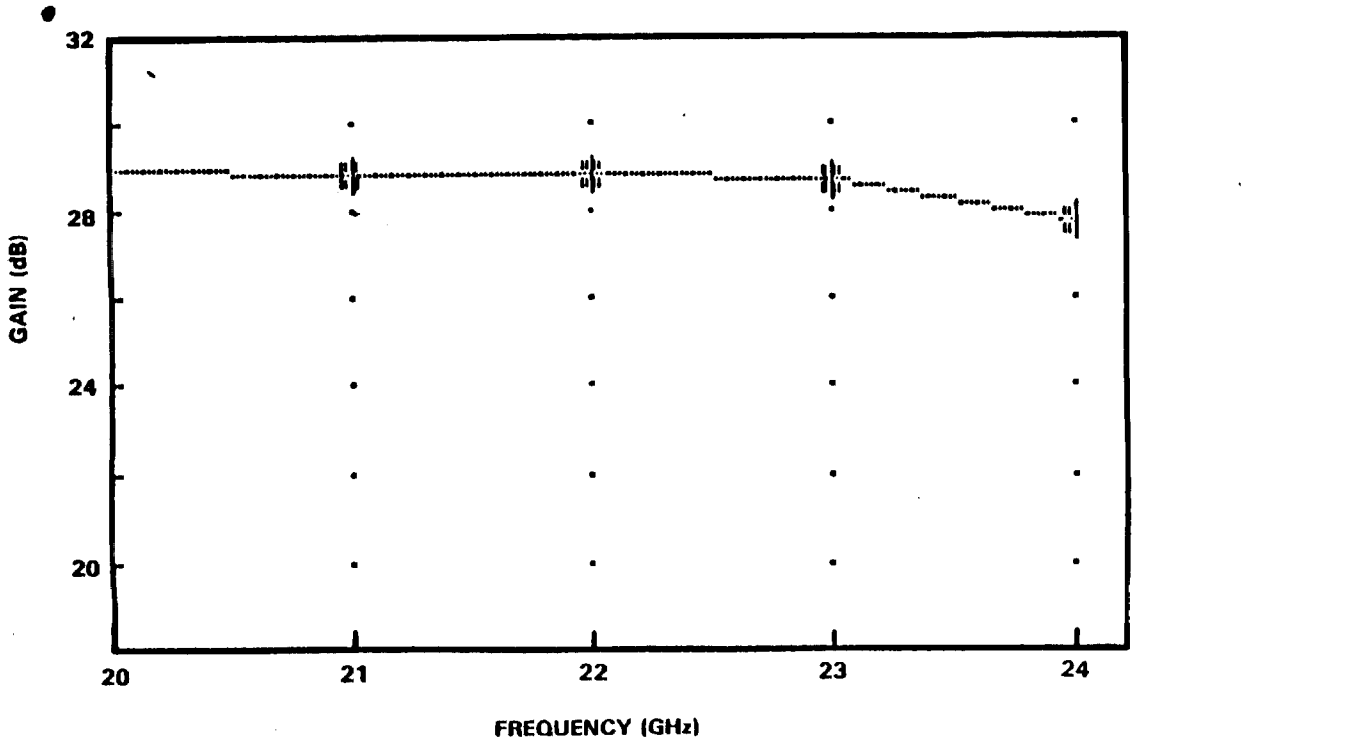


Figure 2-41 Schematic and simulated frequency response of 3-stage 22 GHz LO amplifier.

Figure 2-42 Fabricated chip for 22 GHz LO buffer amplifier.

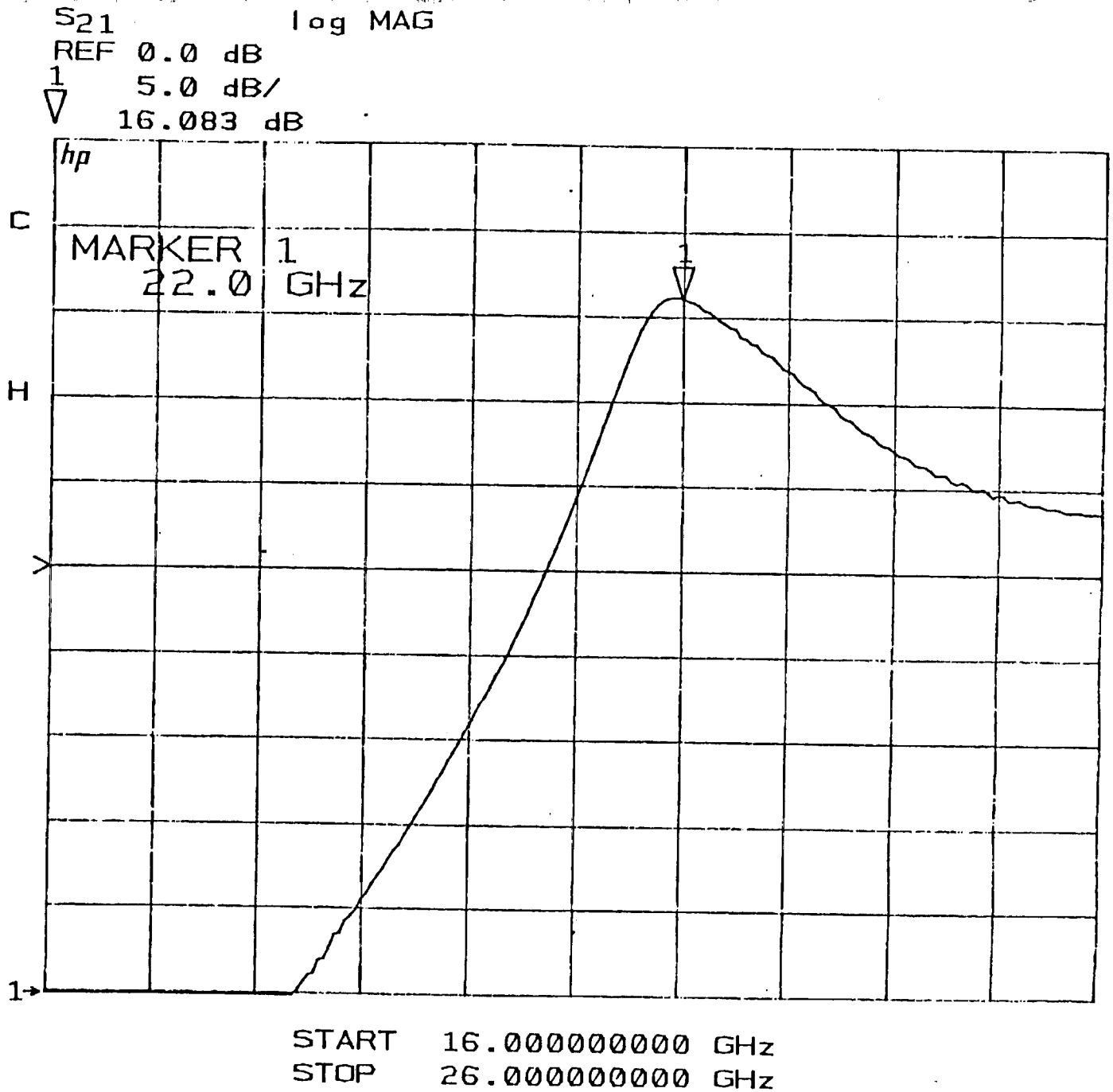


Figure 2-43 Measured gain vs. frequency characteristics for the 3-stage 22 GHz LO buffer amplifier. It had a gain of 16 dB (including fixture losses) at 22 GHz.

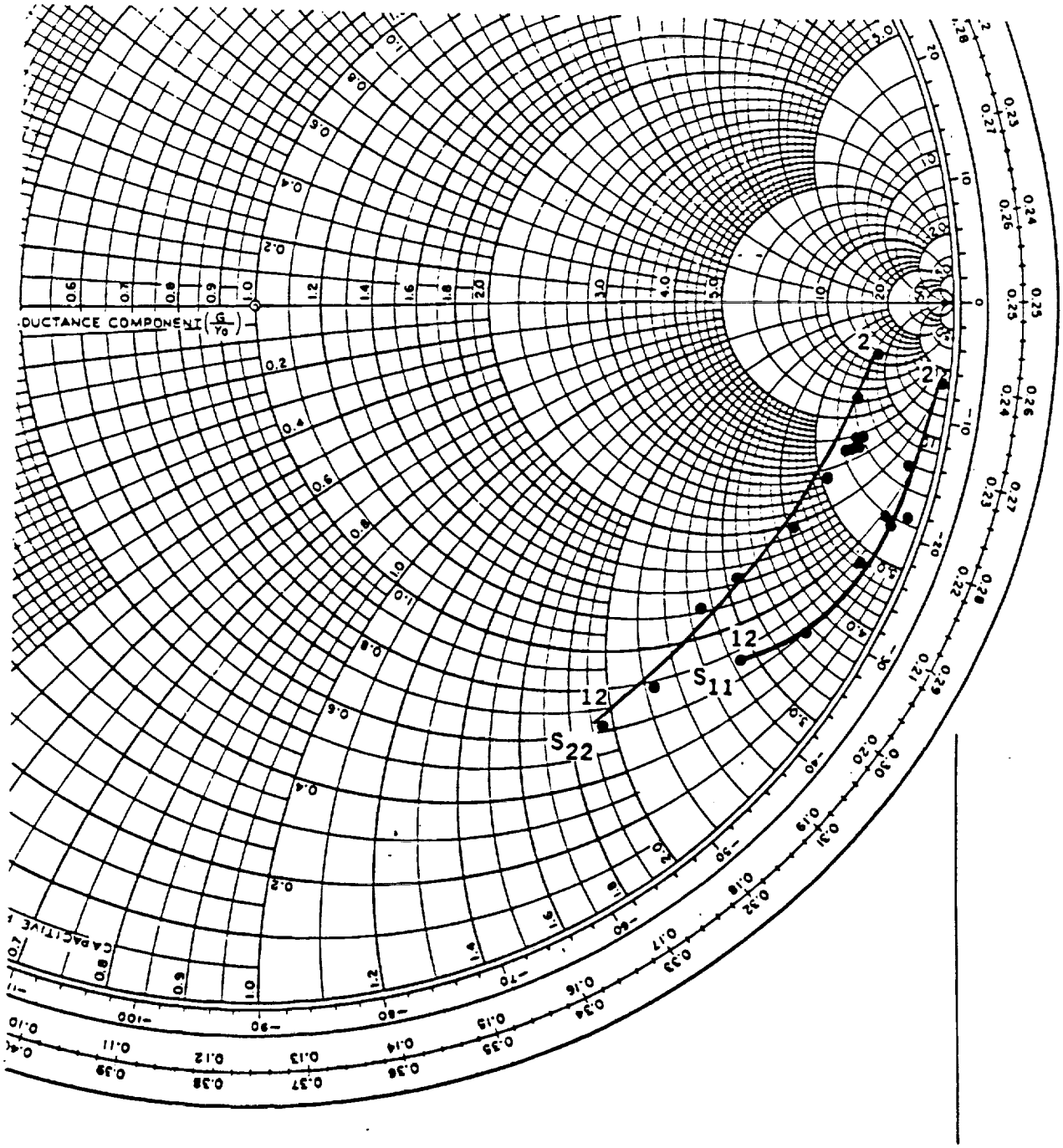


Figure 2-44 Measured S11 and S22 of 0.25 x 100 μm^2 ion implanted device.

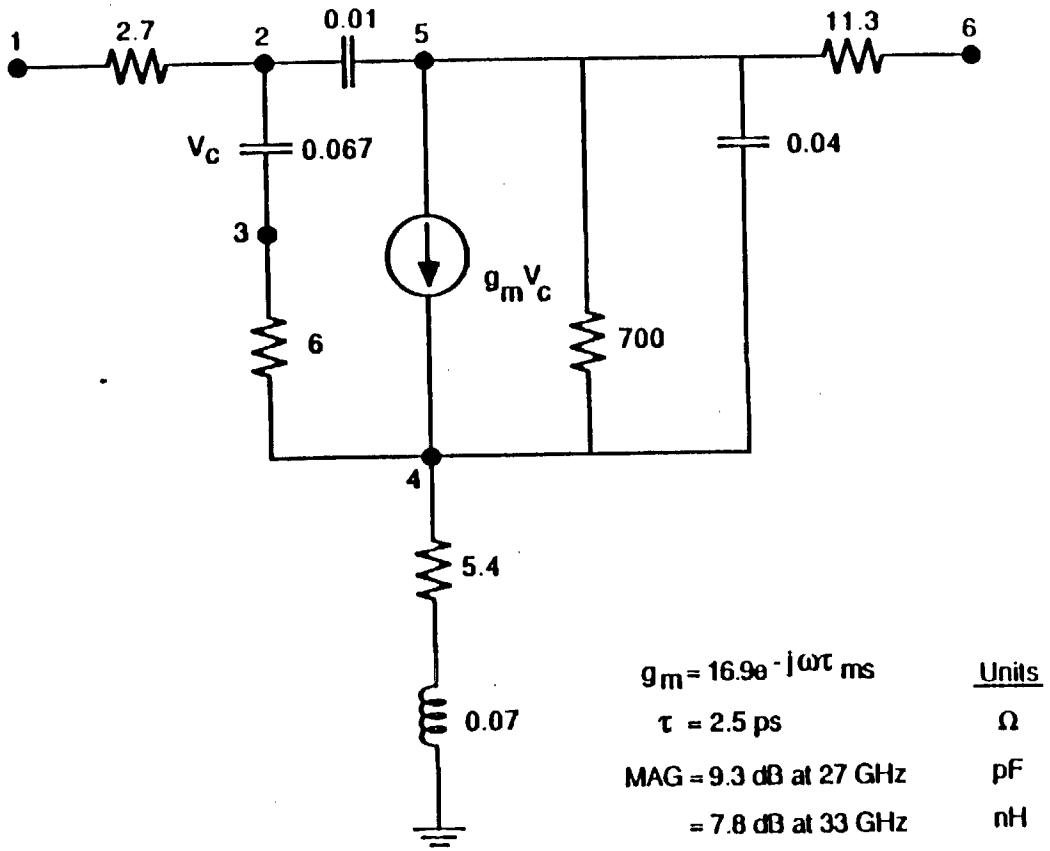
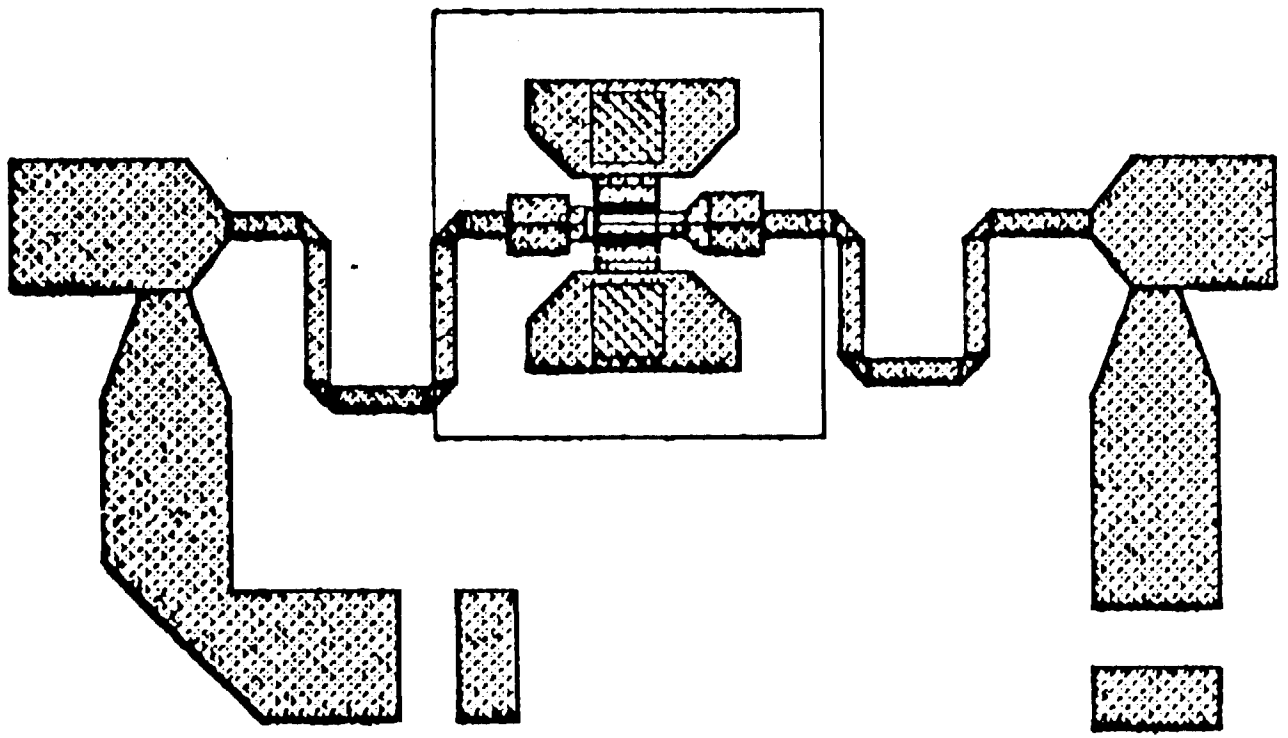
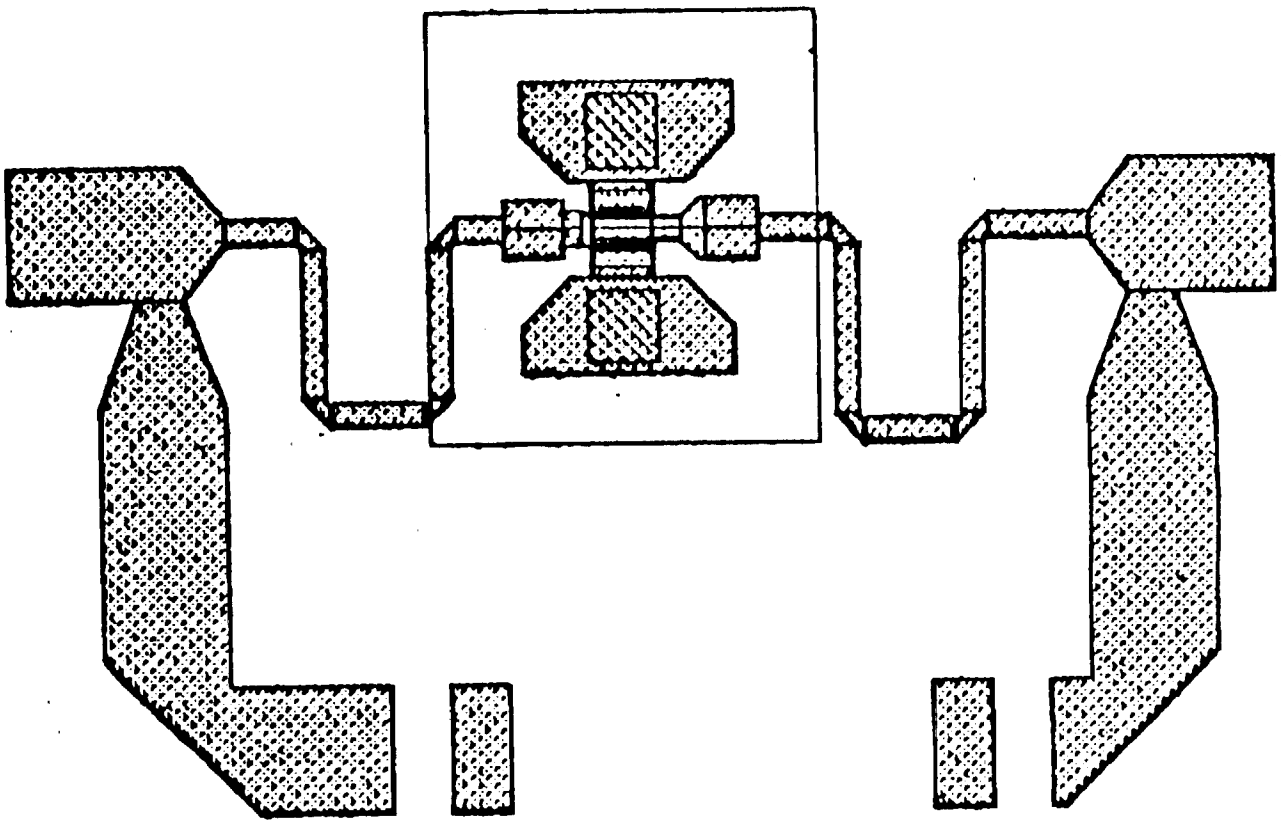


Figure 2-45 Equivalent circuit for 0.25 x 100 μm^2 FET (ion-implanted) at low noise bias.



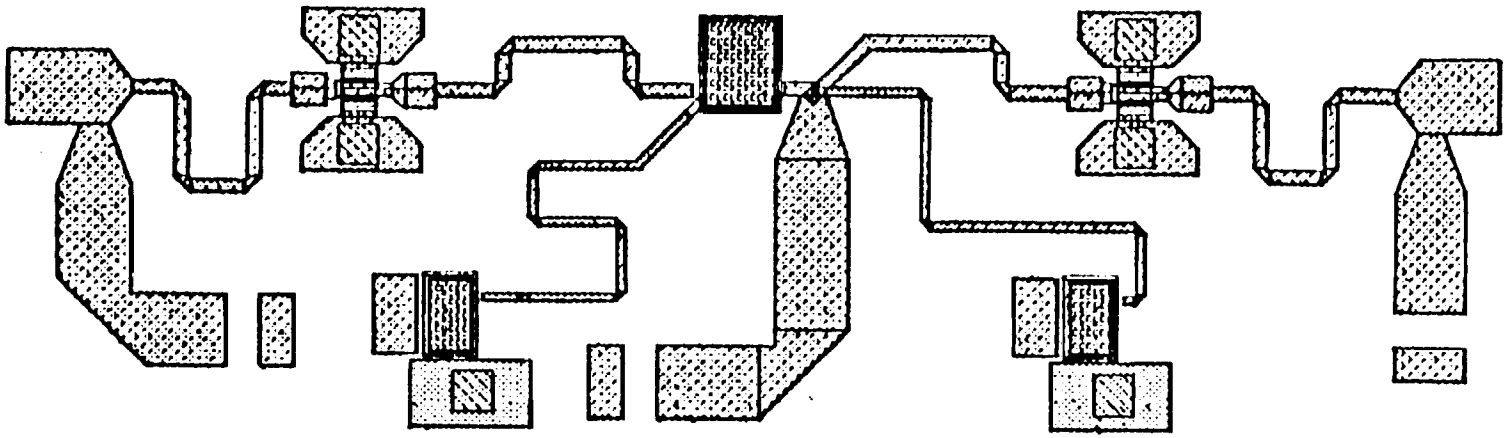
Magnification — 150X

Figure 2-46 (a) LNA1A



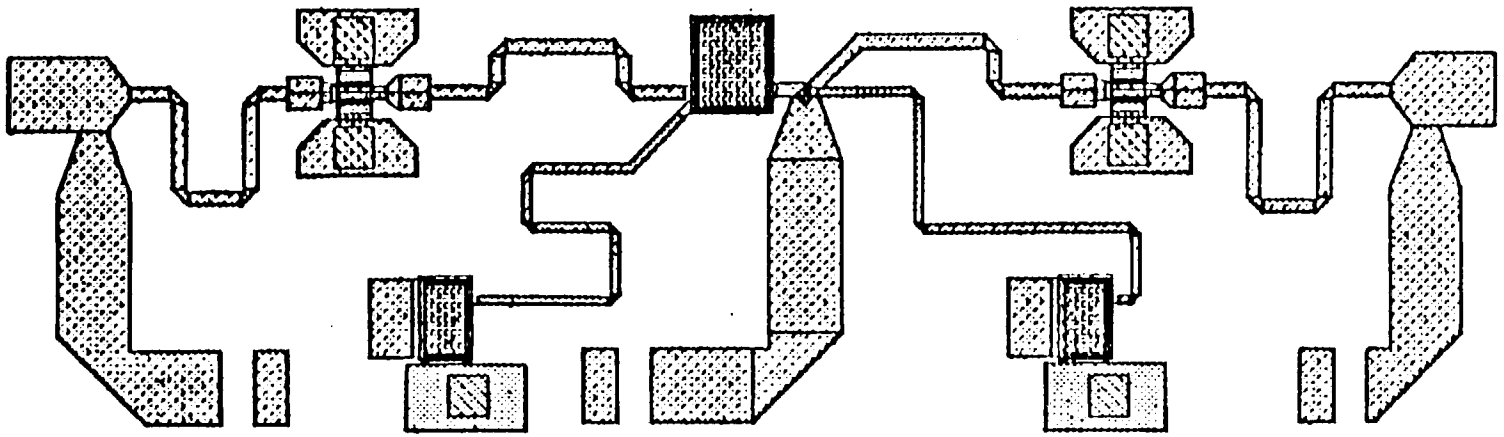
Magnification — 150X

FIGURE 2-46 (b) LNA1B



Magnification — 100X

FIGURE 2-46 (c) LNA2A



Magnification — 100X

FIGURE 2-46 (d) LNA2B.

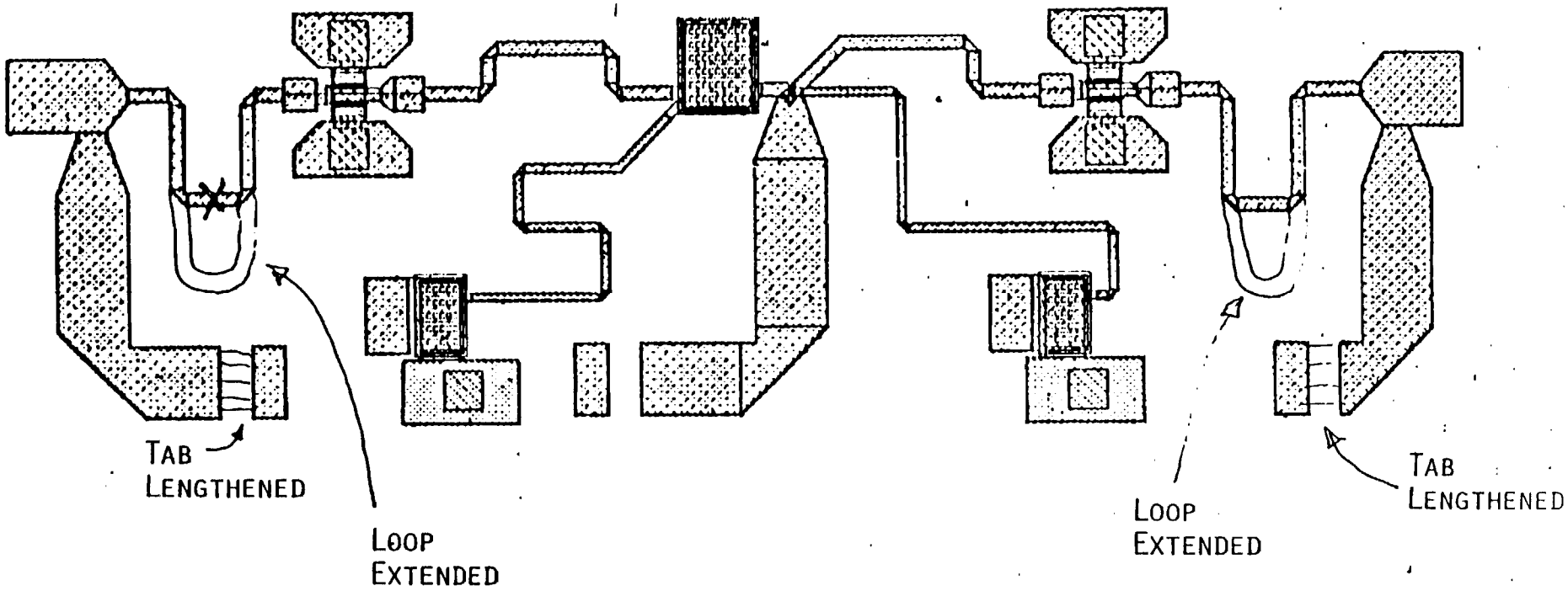
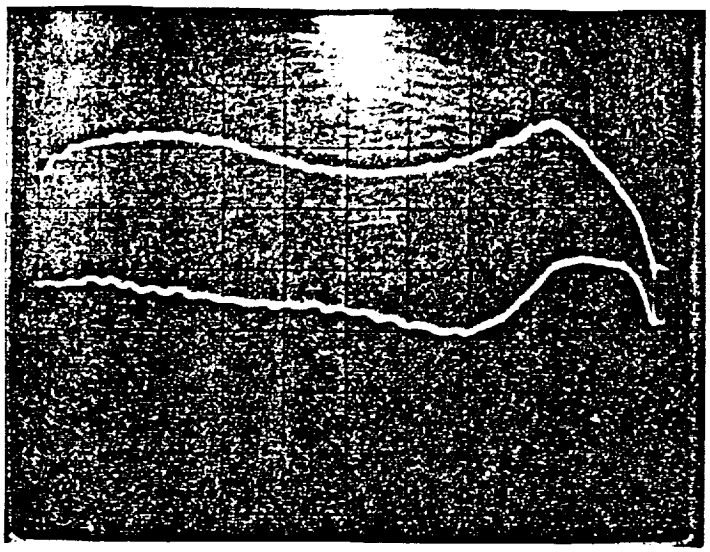


Figure 2-47 On-chip modification on the LNA (LNA2B).



A) UNMODIFIED LNA

GAIN - TOP TRACE

INPUT RETURN LOSS - BOTTOM TRACE

HORIZONTAL 27-37 GHZ

VERTICAL GAIN 5DB/DIV

RETURN LOSS 10DB/DI

CENTERLINE 0DB

BIAS V_{G1} = -0.4V

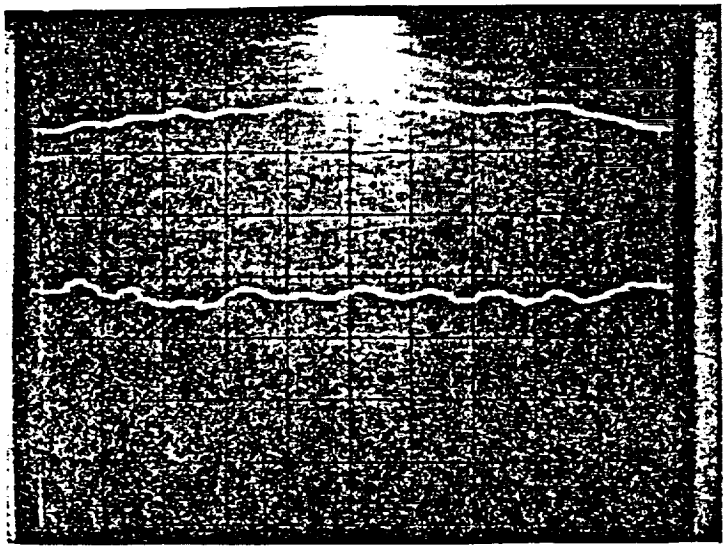
V_{G2} = -1.61V

V_{D1} = 2.7V

V_{D2} = 3.0V

I_{D1} = 37.5 MA

I_{D2} = 23.2 MA



B) LNA AFTER MODIFICATION

GAIN - TOP TRACE

RETURN LOSS - BOTTOM TRACE

HORIZONTAL 27.5-30 GHZ

VERTICAL GAIN -5DB/D

RETURN LOSS 10DB/D

BIAS V_{G1} = -.64V

V_{G2} = -1.94V

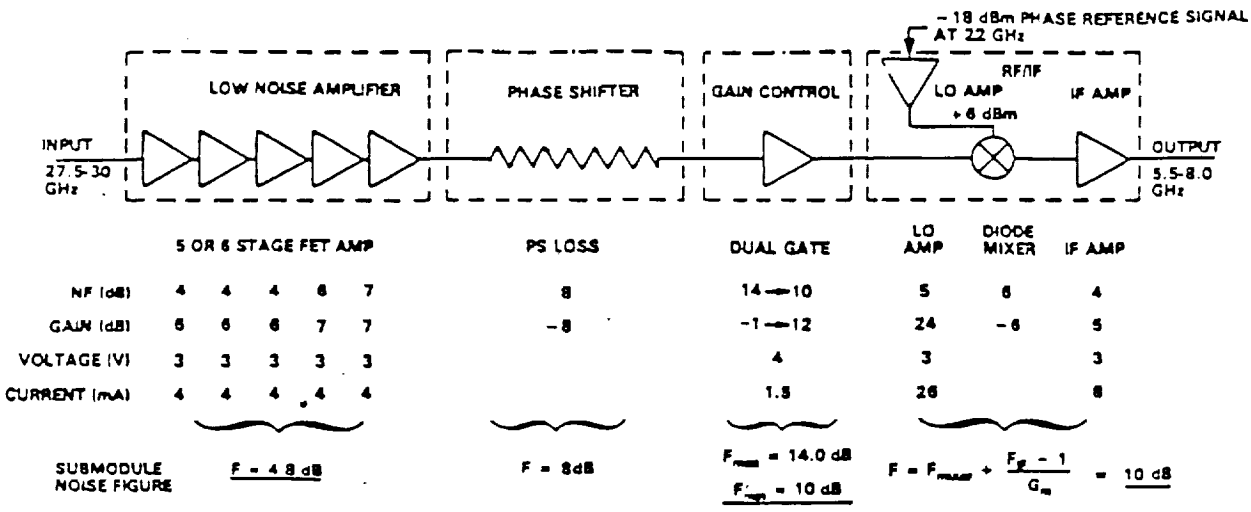
V_{D1} = 3.49V

V_{D2} = 2.70V

I_{D1} = 34 MA

I_{D2} = 23.3 MA

Figure 2-48 LNA response before and after the modification.



Overall Performance

Noise Figure: 4.9 dB (Max Gain); 5.0 (Min Gain)
RF/IF Conversion Gain: 35 dB (max Gain); 23 dB (Min Ga
Minimum Detectable Signal: -70 dBm
Dynamic Range: 30 dB minimum

Figure 2-49 Interconnected receiver goal.

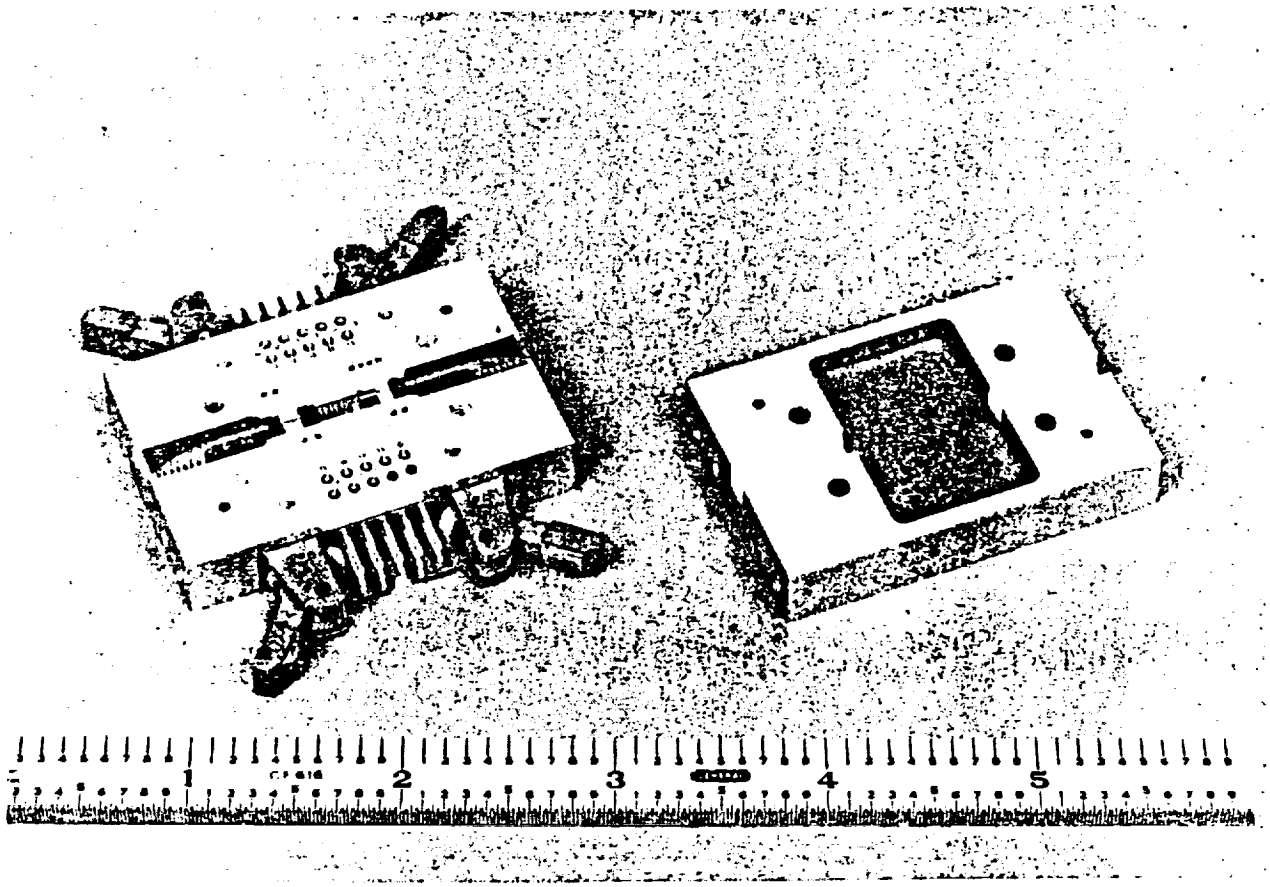


Figure 2-50 Three chip receiver assembled in single house with cover removed. The housing has finline-w/g transitions at the input and the output.

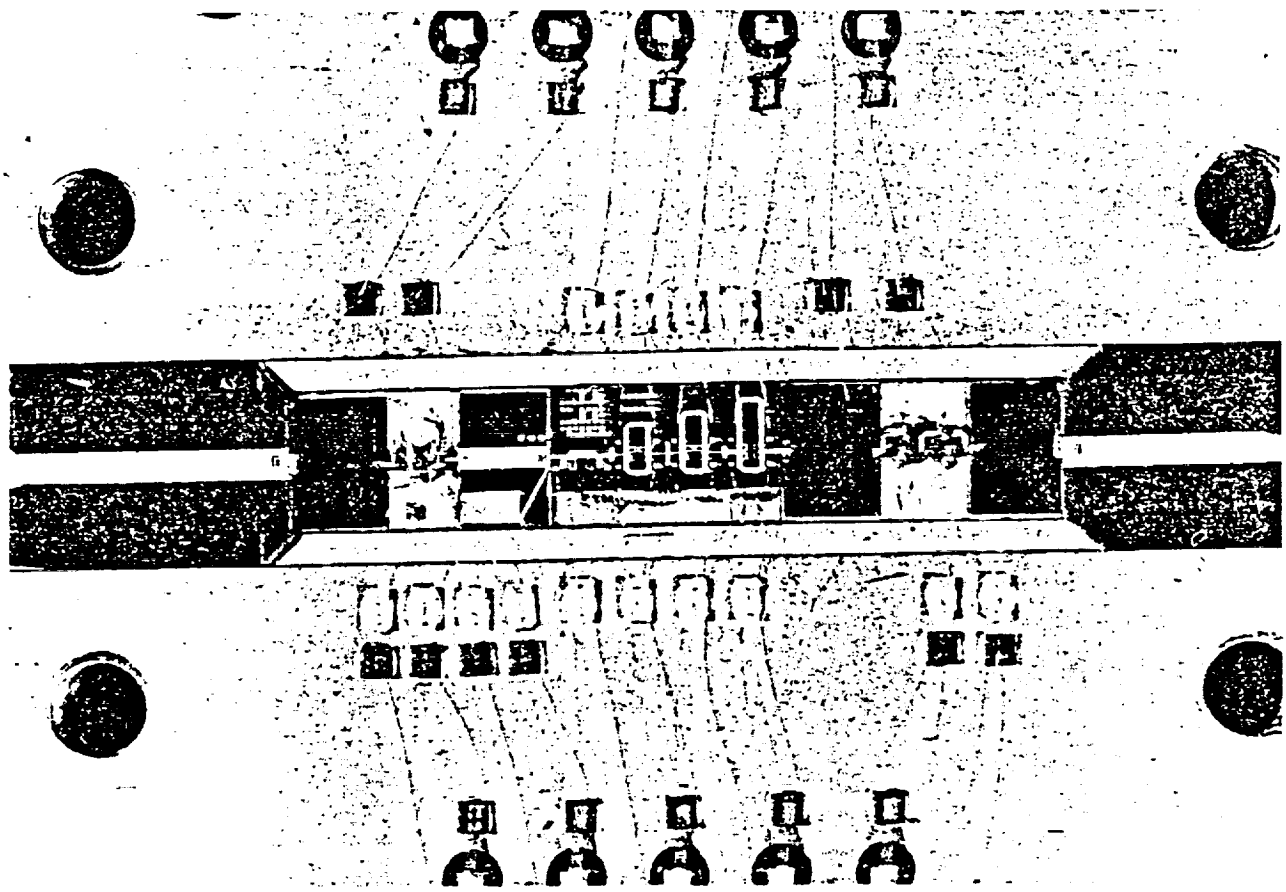


Figure 2-51 Close up view of assembled receiver.

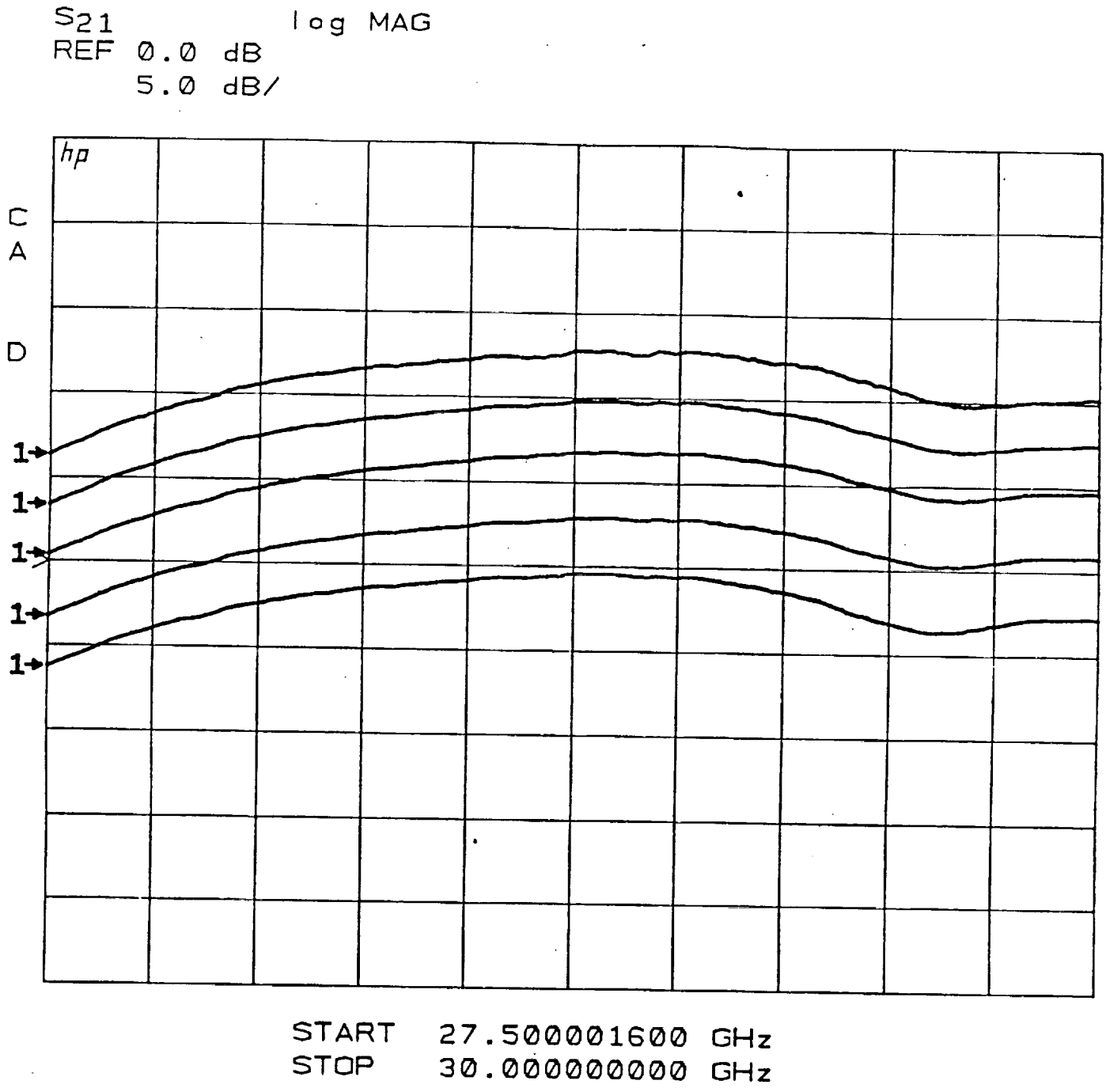


Figure 2-52 Interconnected receiver gain characteristics

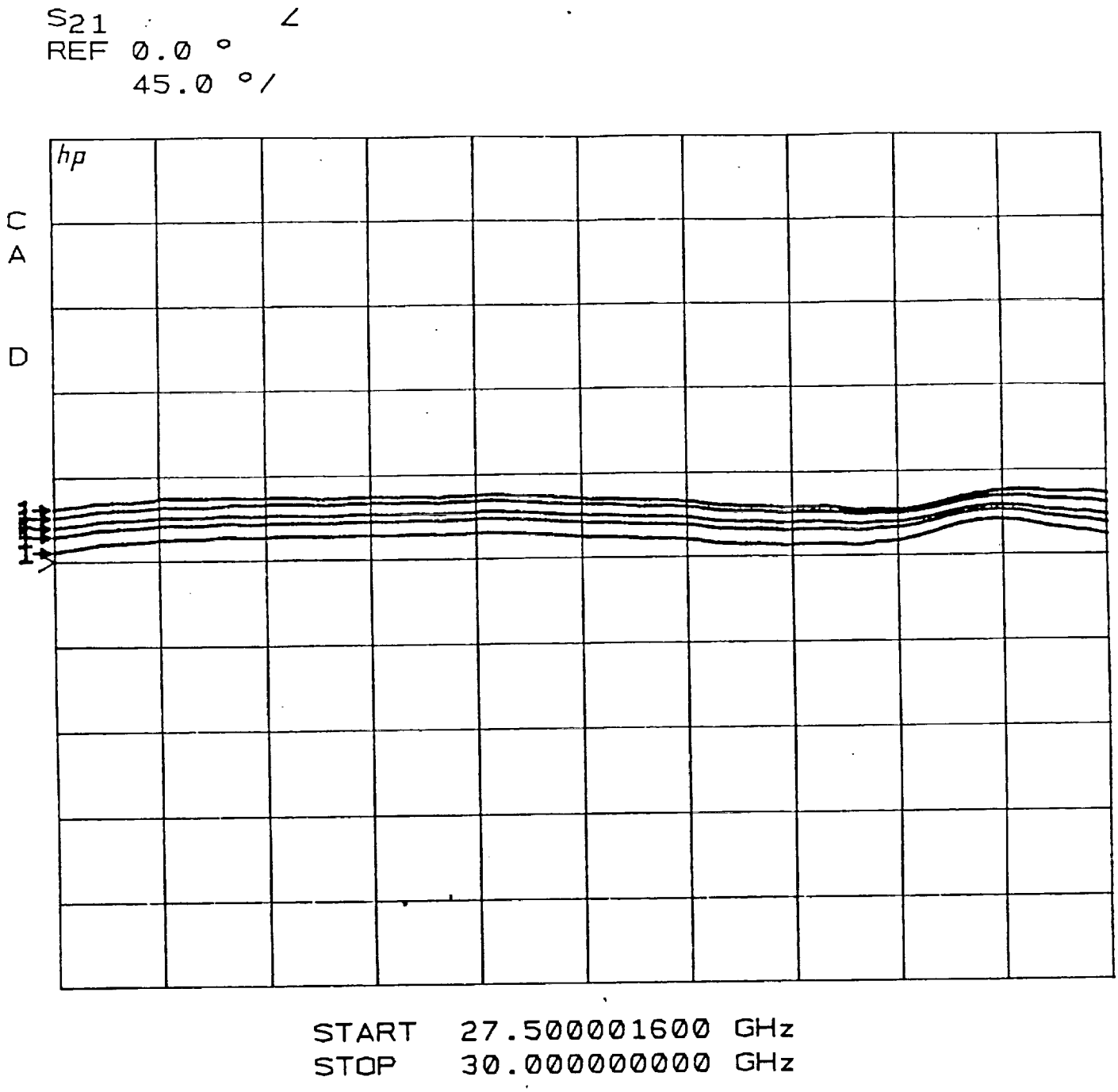


Figure 2-53 Phase envelope of the interconnected receive module at five gain settings. The worst case occurred at the band edges (± 12°).

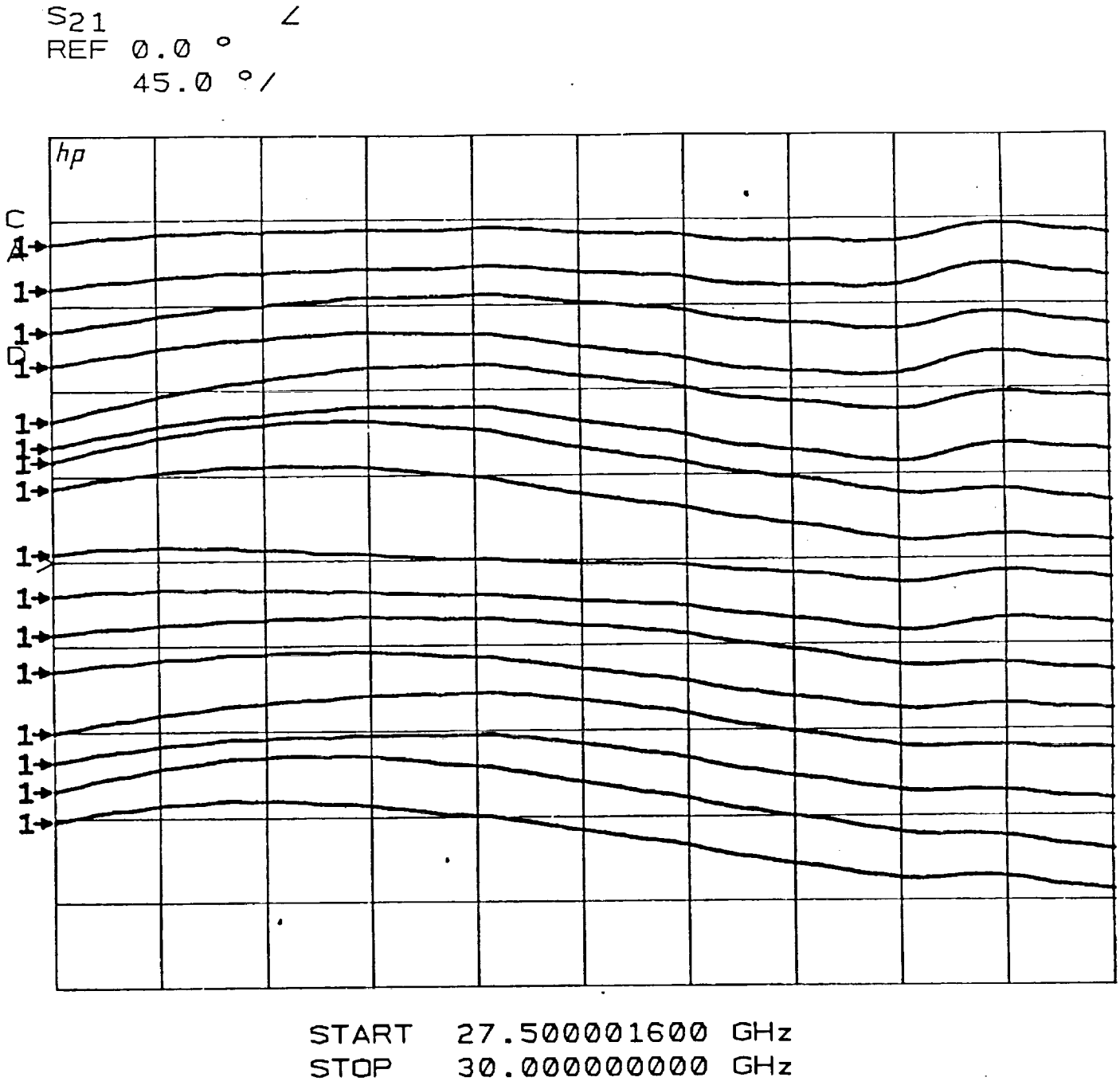


Figure 2-54 Differential phase shift for sixteen states of the interconnected receive module.

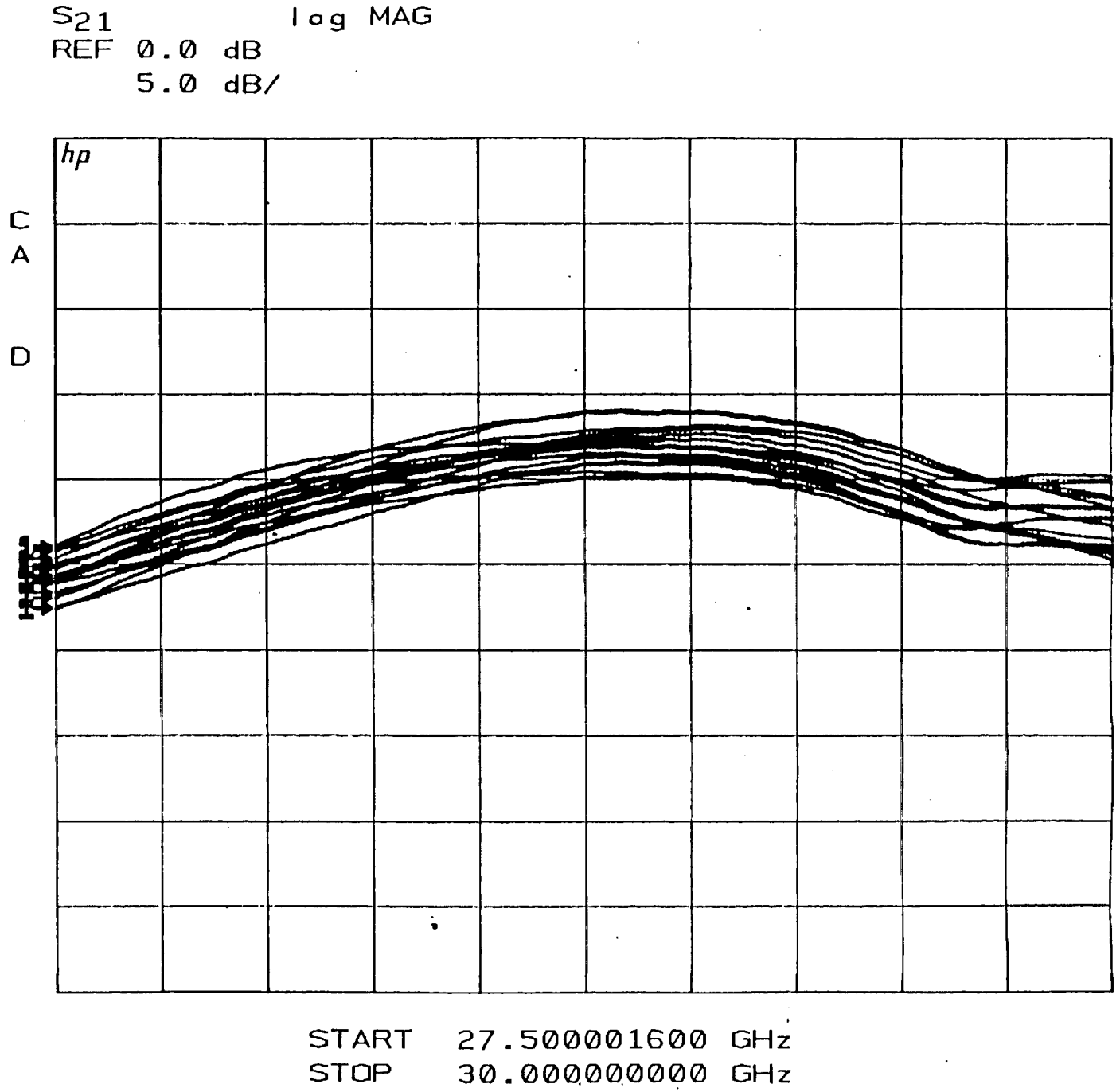


Figure 2-55 The insertion gain envelope for the sixteen states of the receive module.

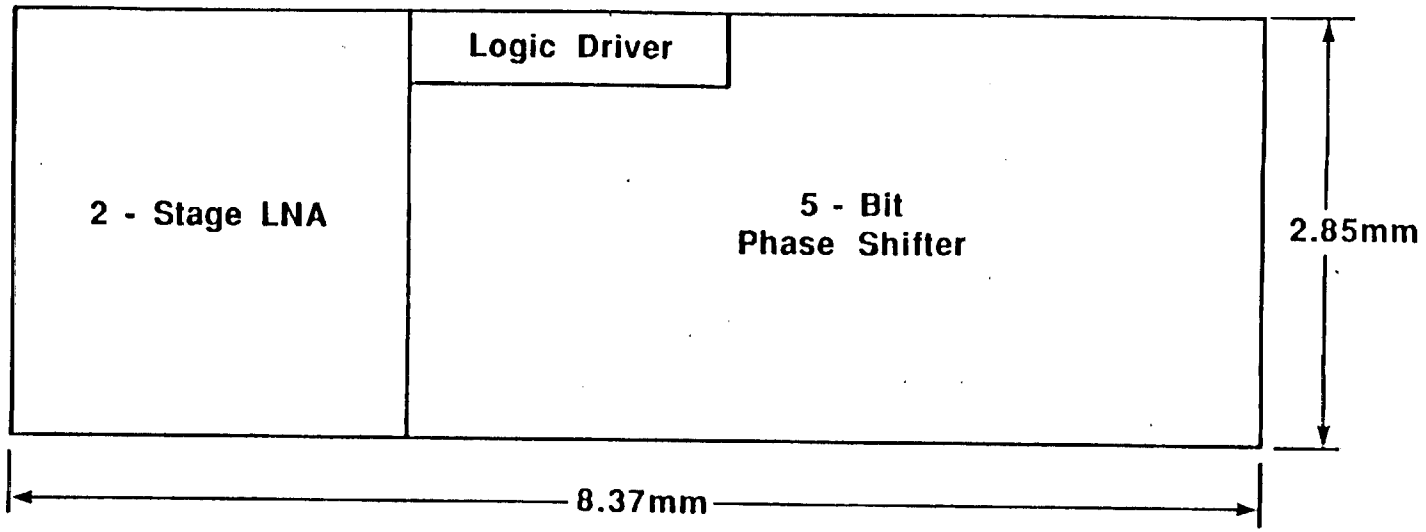
Table 2-1 The noise figure data of the interconnected receiver module.

RECEIVER NOISE FIGURE DATA

f = 28.75 GHz

GAIN SETTING	NOISE FIGURE
"12 dB"	14.0 dB
" 9 dB"	14.8 dB
" 6 dB"	15.7 dB
" 2 dB"	17.2 dB
"-1 dB"	18.5 dB

Figure 2-56 Complete reticle layout of the monolithic CTS receiver.



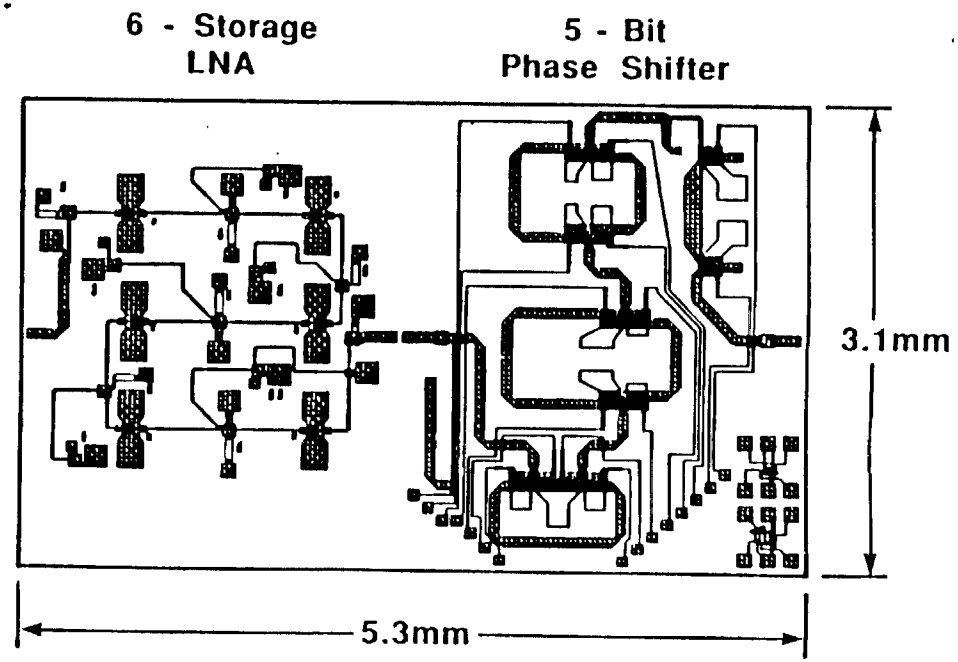


Figure 2-57 LNA/phase shifter combination with reduced size phase shifter.

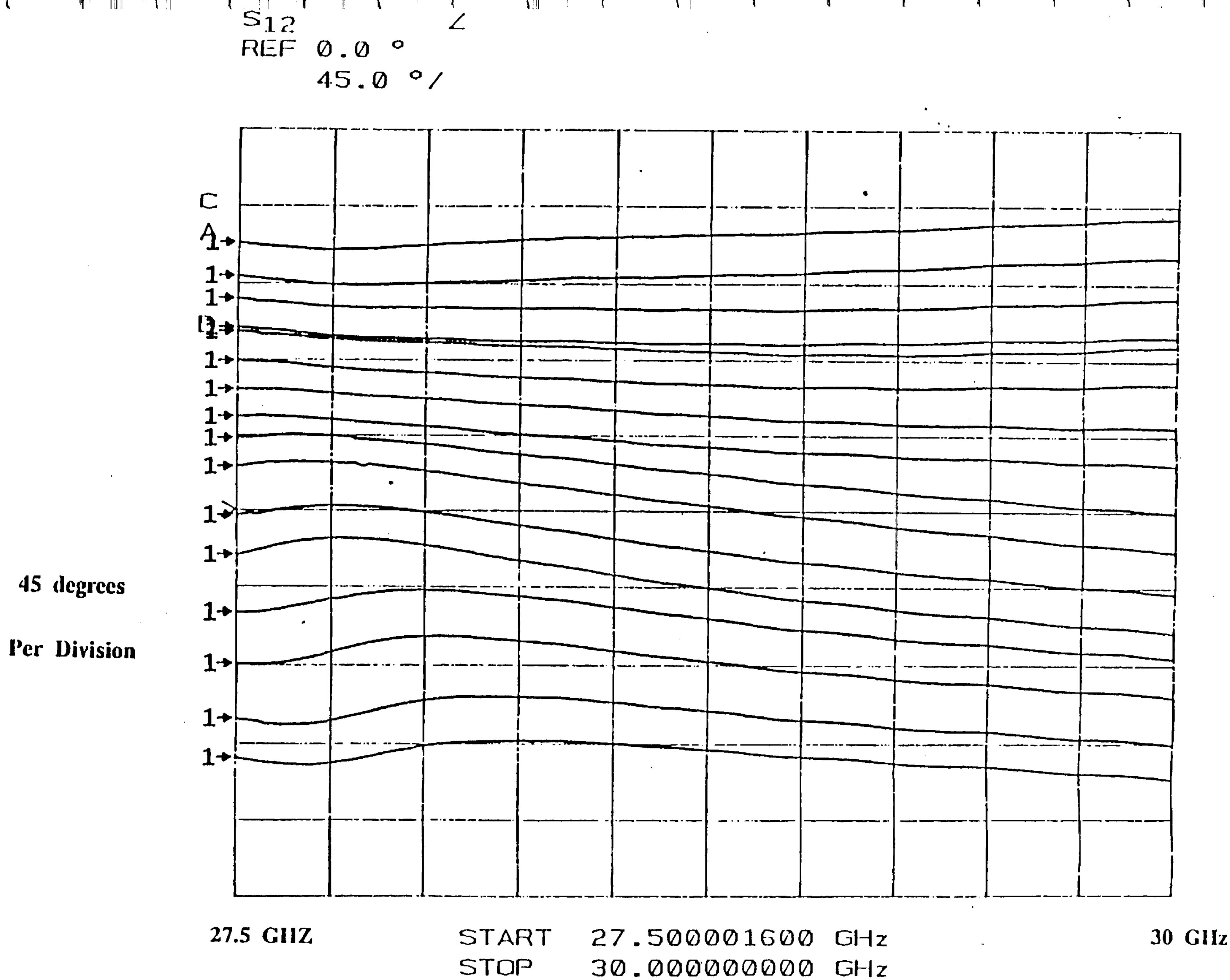
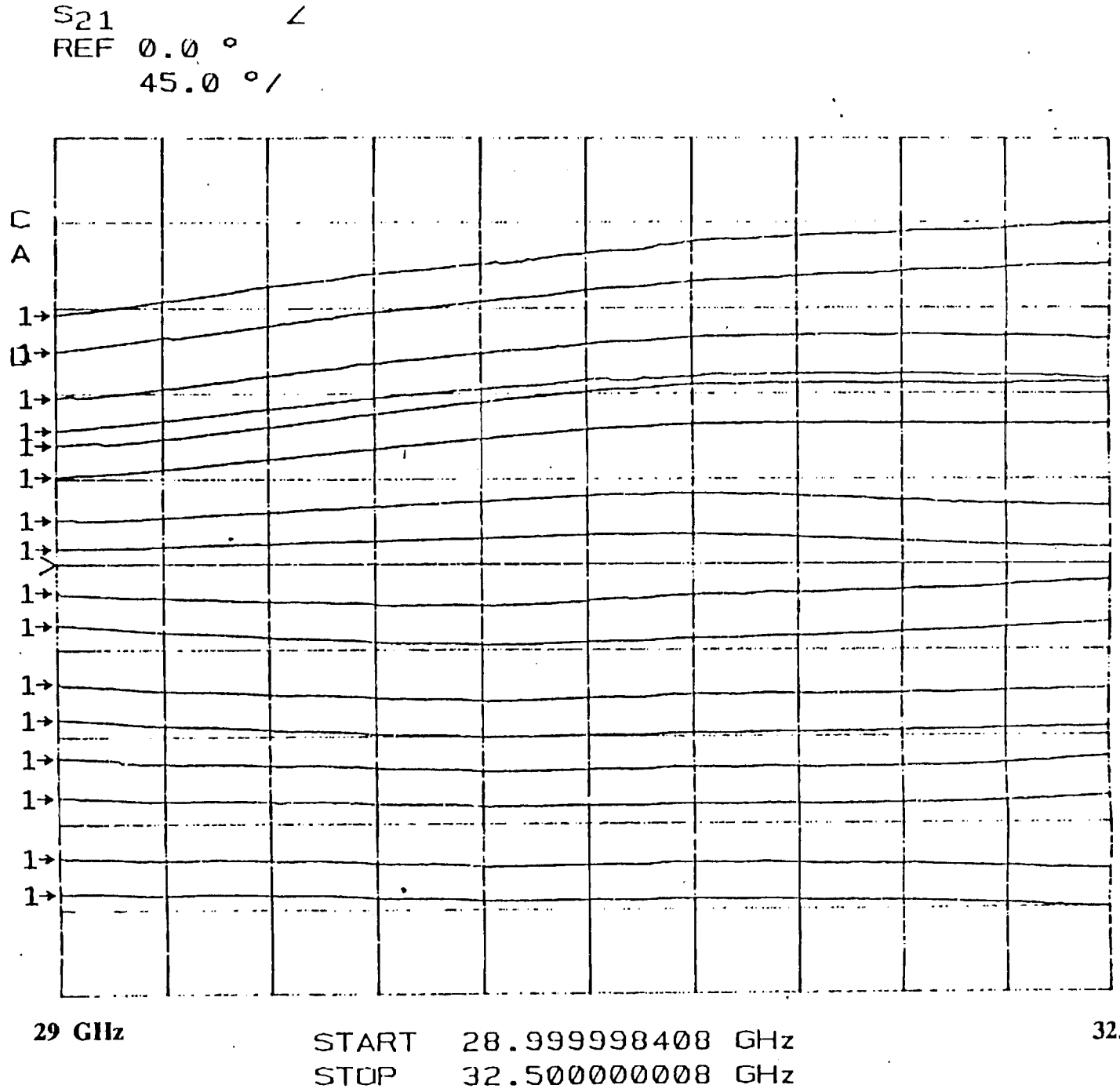


Figure 2-58 Reduced size phase shifter performance in the NASA band.



45 Degrees Per Division

29 GHz **32.5 GHz**

Figure 2-59 Phase shifter performance in the best frequency range of operation.

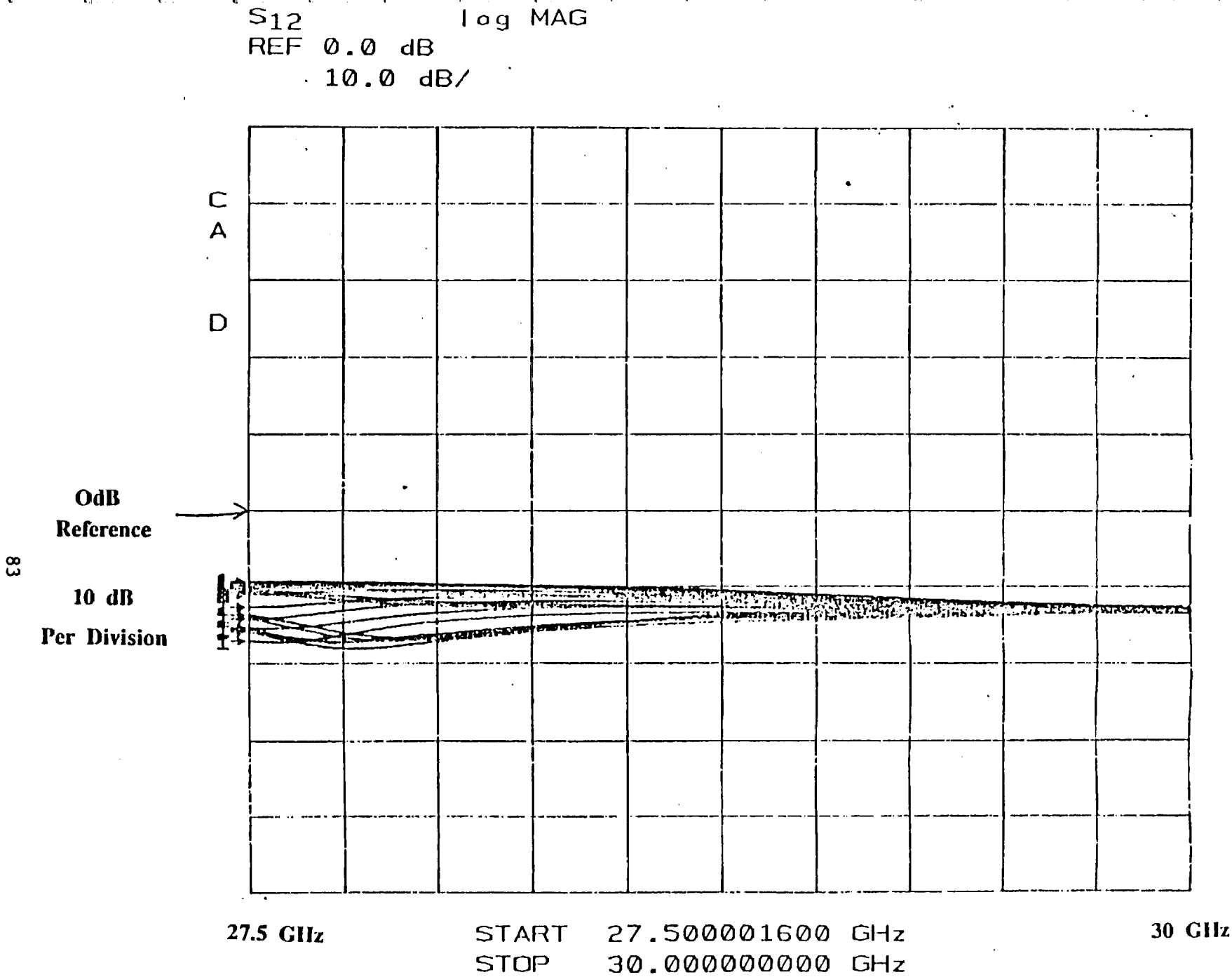


Figure 2-60 Insertion loss envelope in NASA bands.

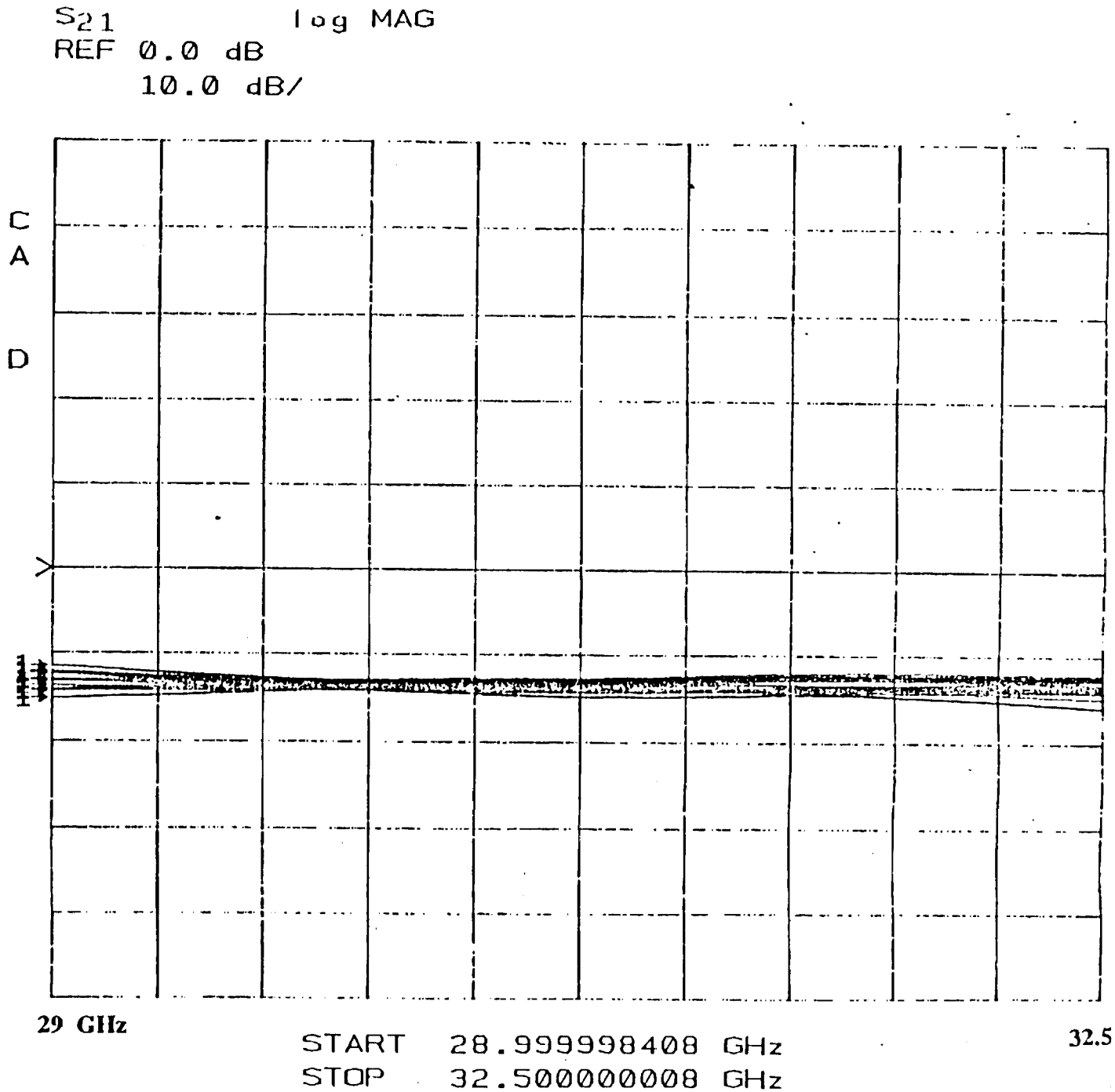


Figure 2-61 Insertion loss envelope in the best frequency range of operation.

Figure 2-62 (a) Photograph of the on-chip logic circuits for controlling phase bits.

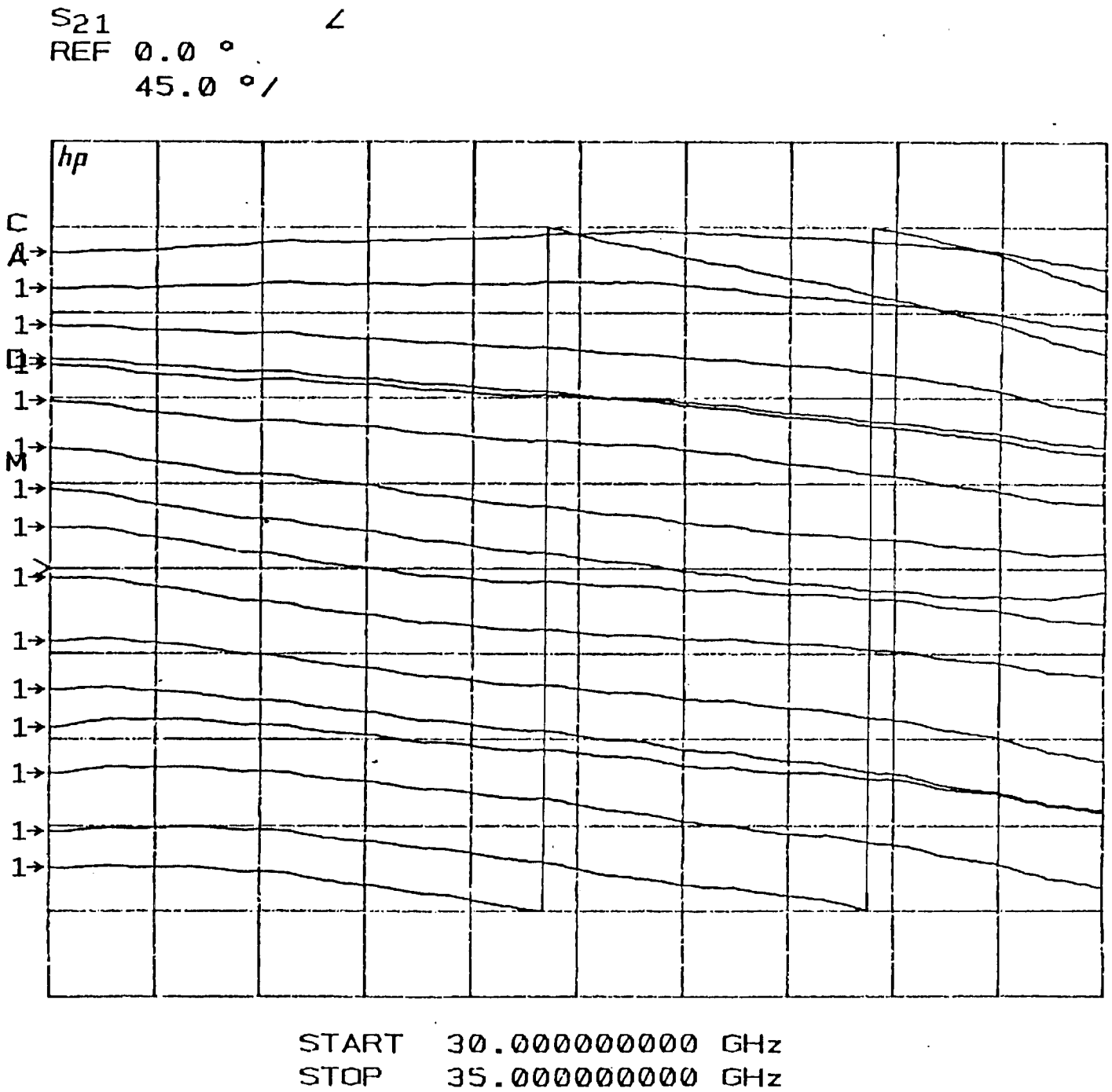


FIGURE 2-62 (b) Phase characteristics with 180° bit switched by on-chip logic.

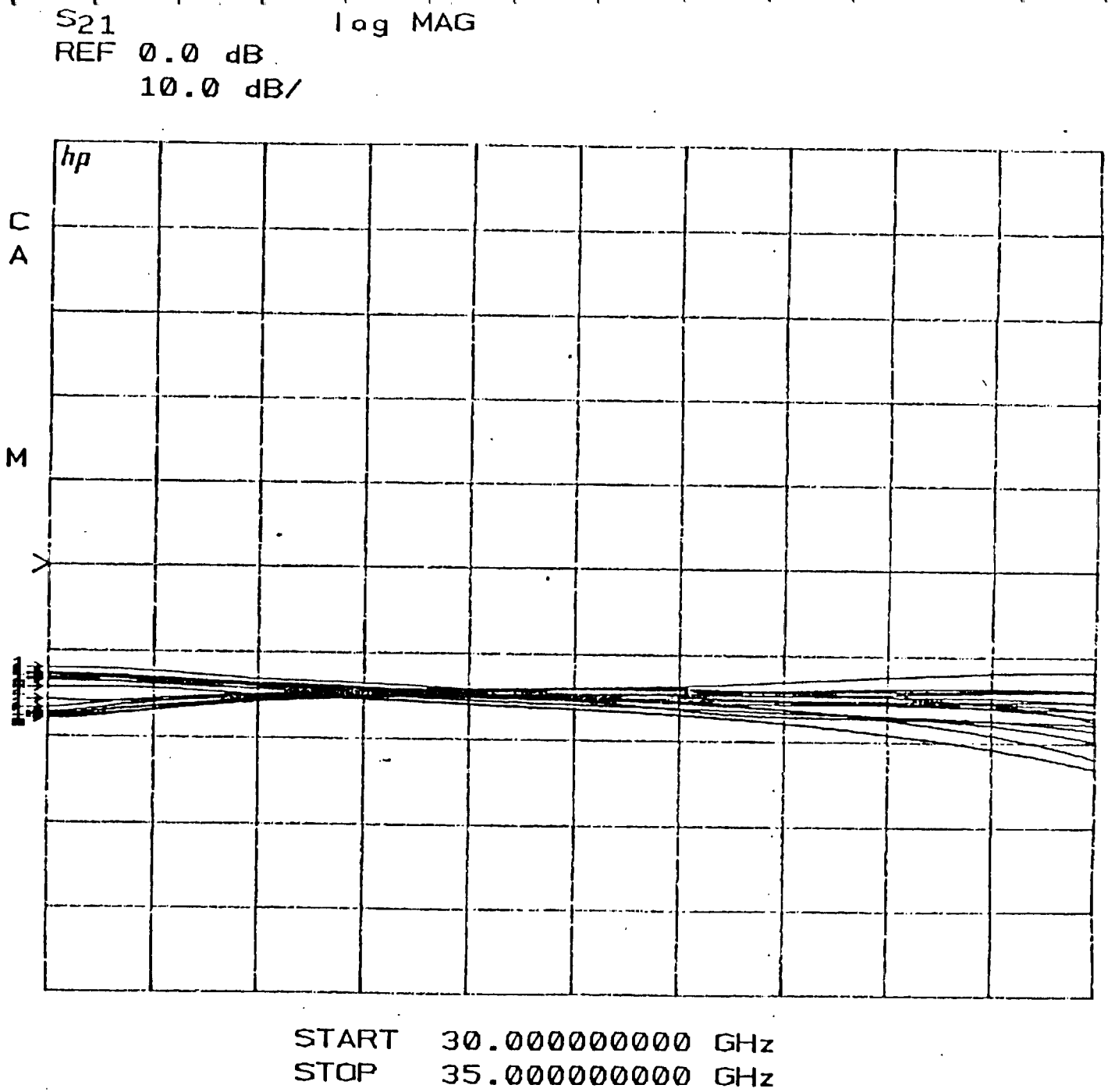


FIGURE 2-62 (c) Insertion loss envelope with 180° bit switched by on-chip logic.

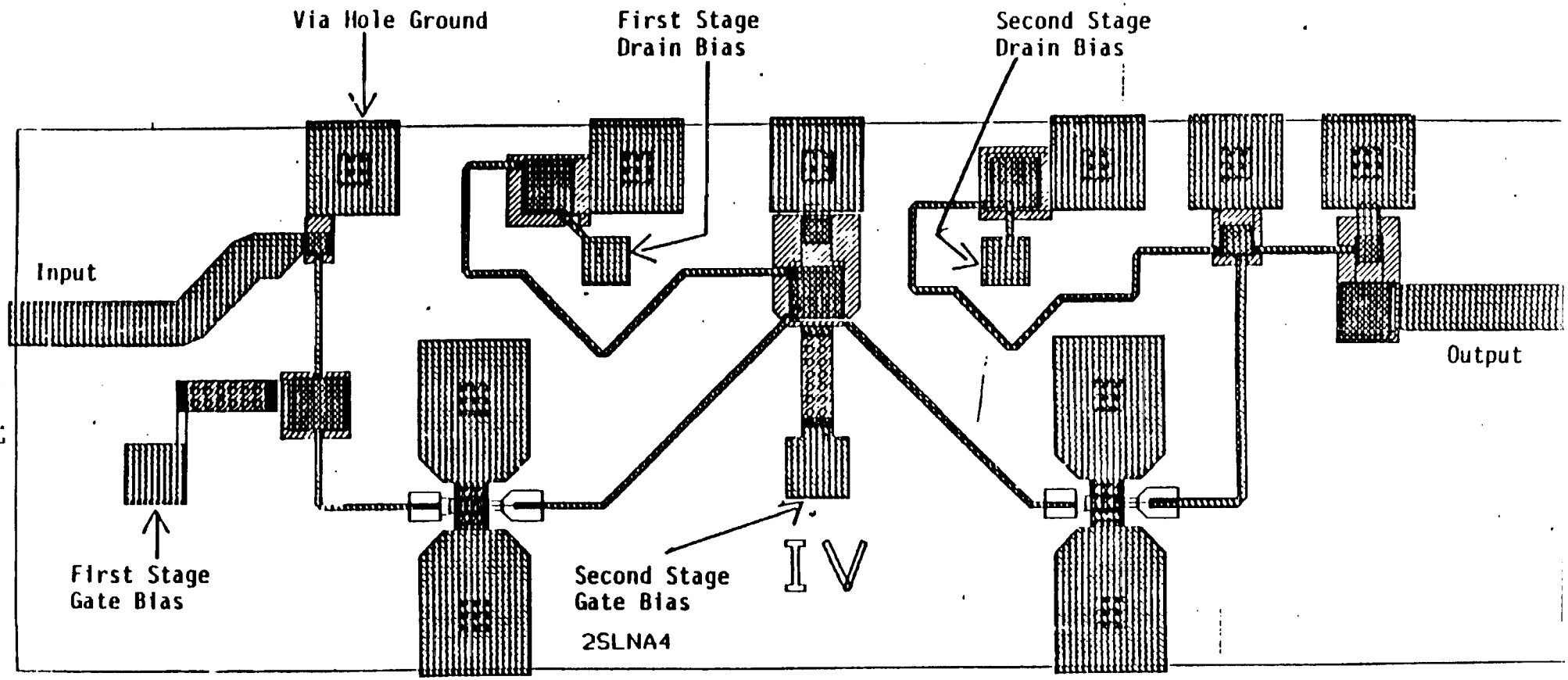


Figure 2-63 2-stage LNA on 4-mil GaAs.

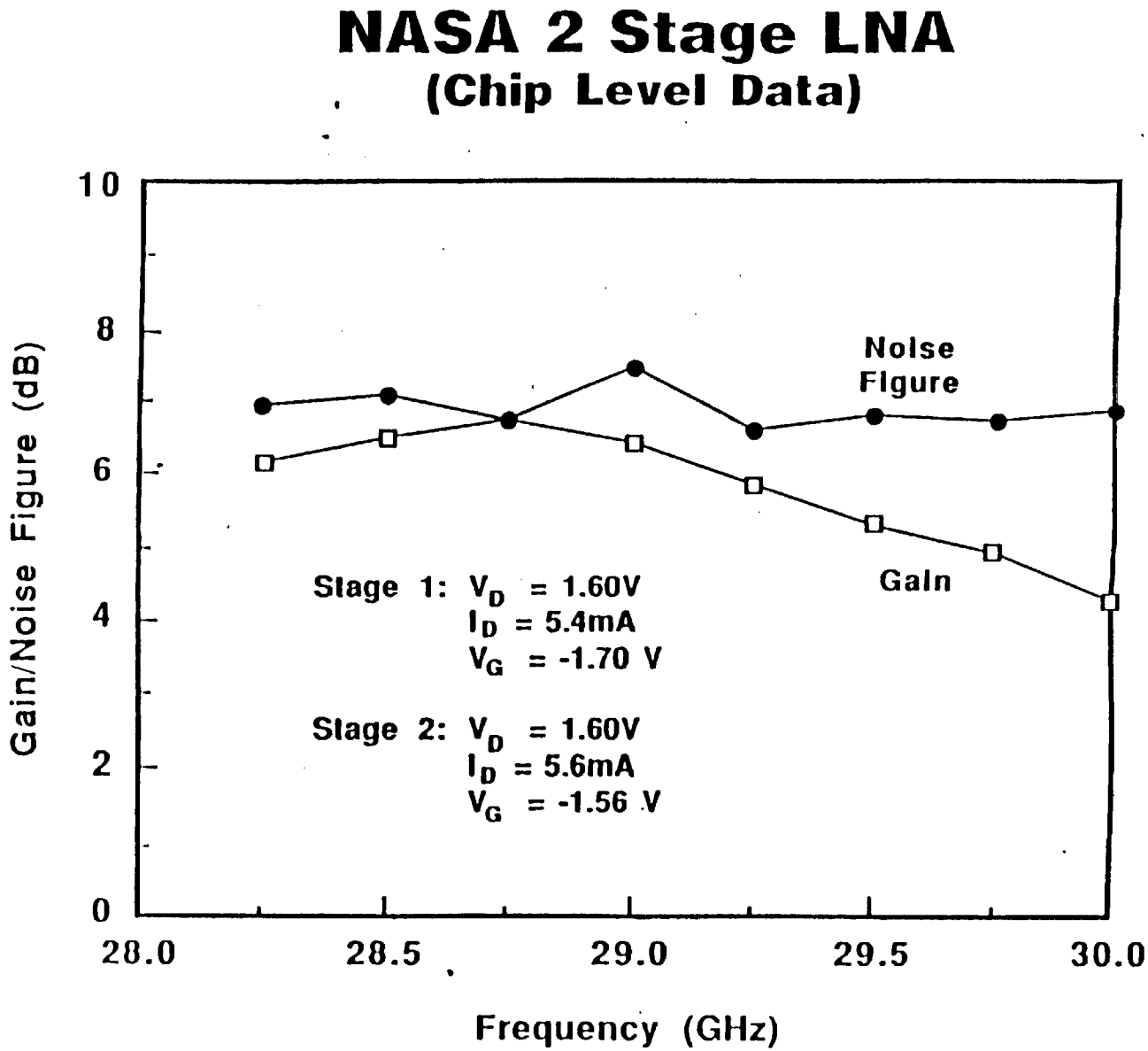
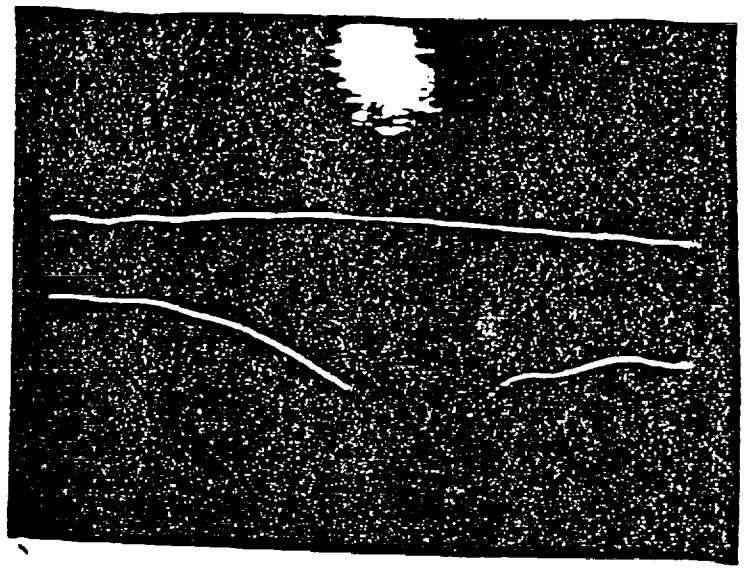


Figure 2-64 2-stage LNA gain and noise figure performance.

Horizontal 27.5-30 GHz
Reference - 0dB Center Line

Gain (top trace)
5 dB/div

Input Return Loss
10 dB/div

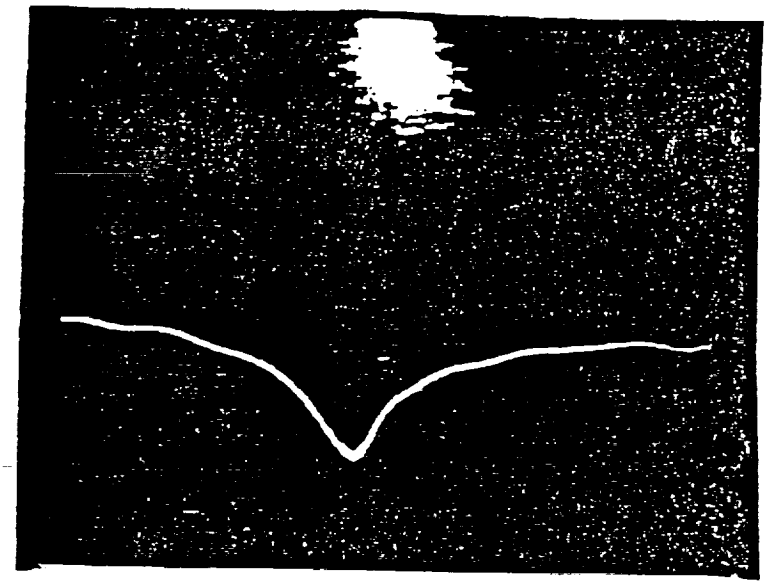


a) Gain and Input Return Loss

Horizontal 27.5-30GHz

Reference - 0dB Center Line

Output Return Loss
10 dB/div



b) Output Return Loss

Figure 2-65 Gain and return loss data for the 2-stage LNA over NASA band.

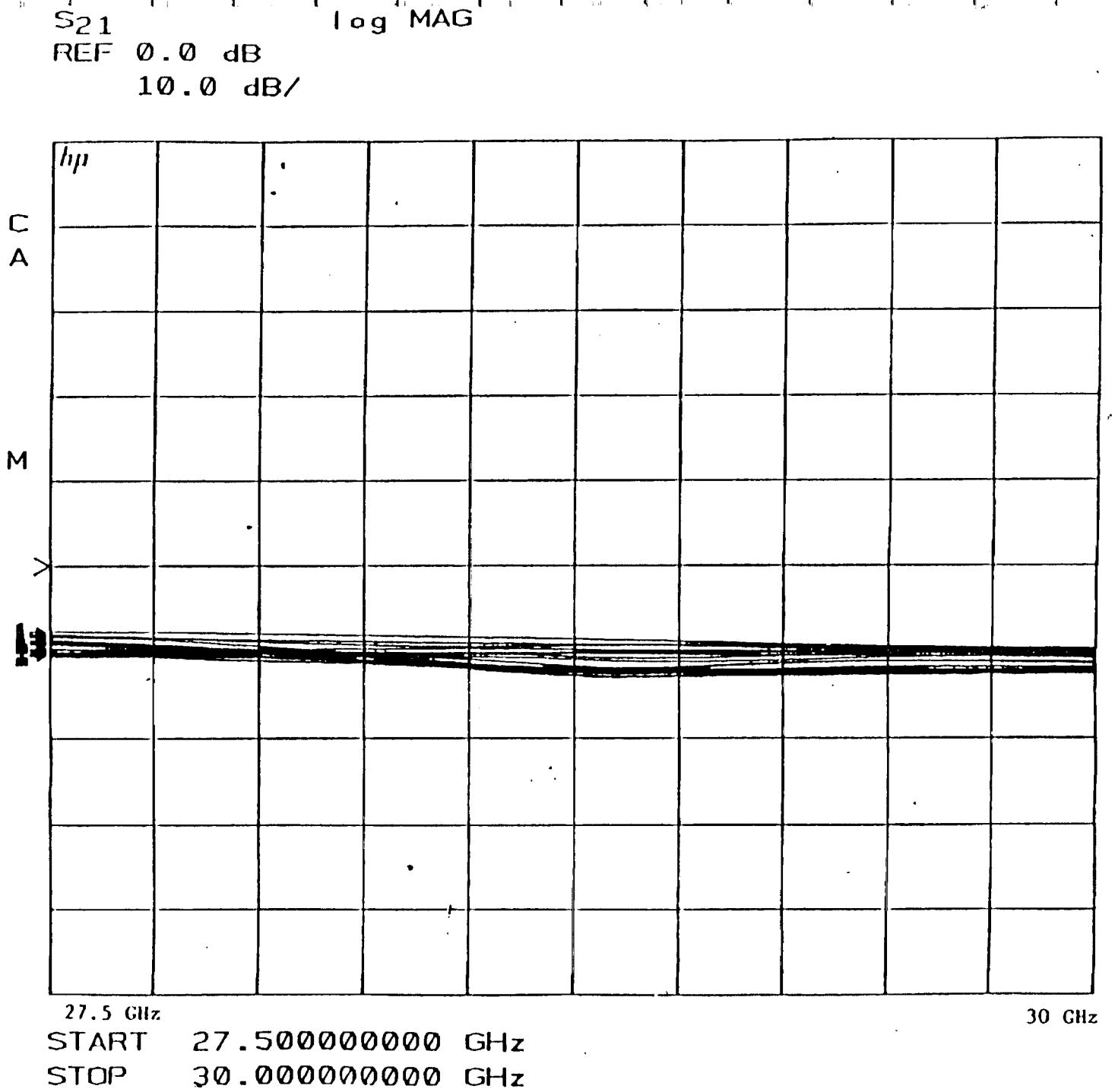


Figure 2-66 Insertion loss envelope for the phase shifter after cutting the control line over the transmission line.

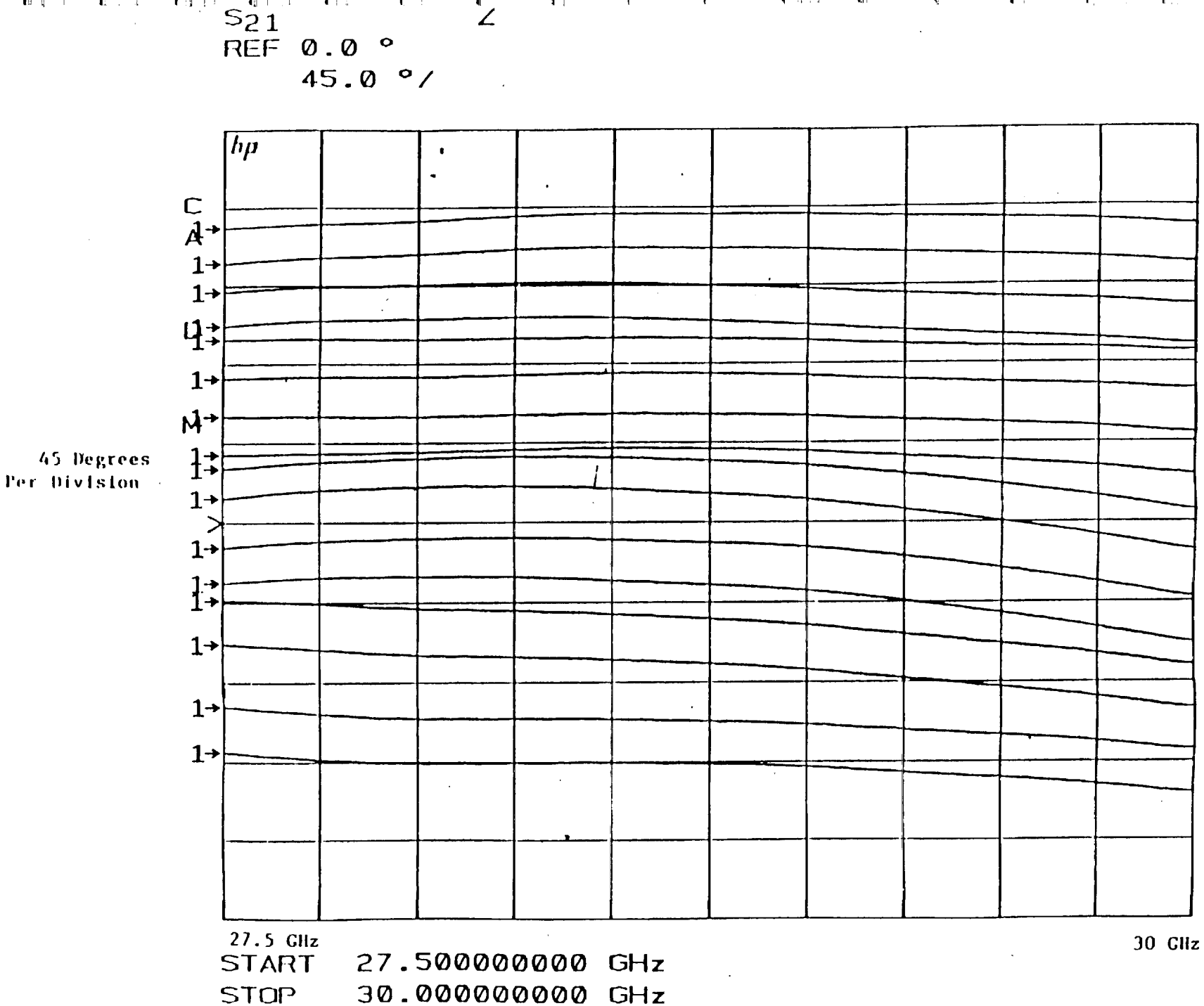


Figure 2-67 Phase states for the phase shifter after cutting the dc control lines over the transmission line.

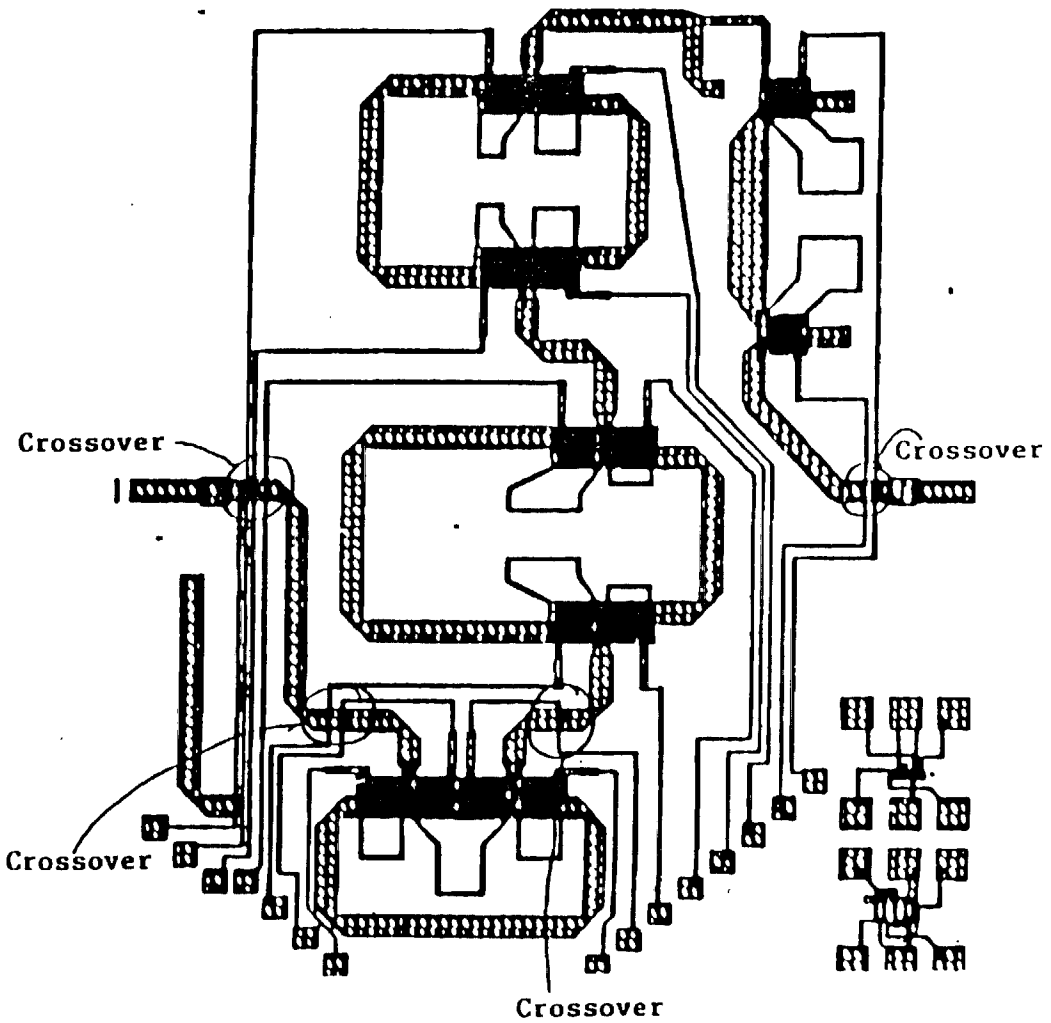


Figure 2-68 The modifications that were carried out by the control lines are shown. The control lines were cut to reduce the coupling between the dc control line and the RF transmission line.

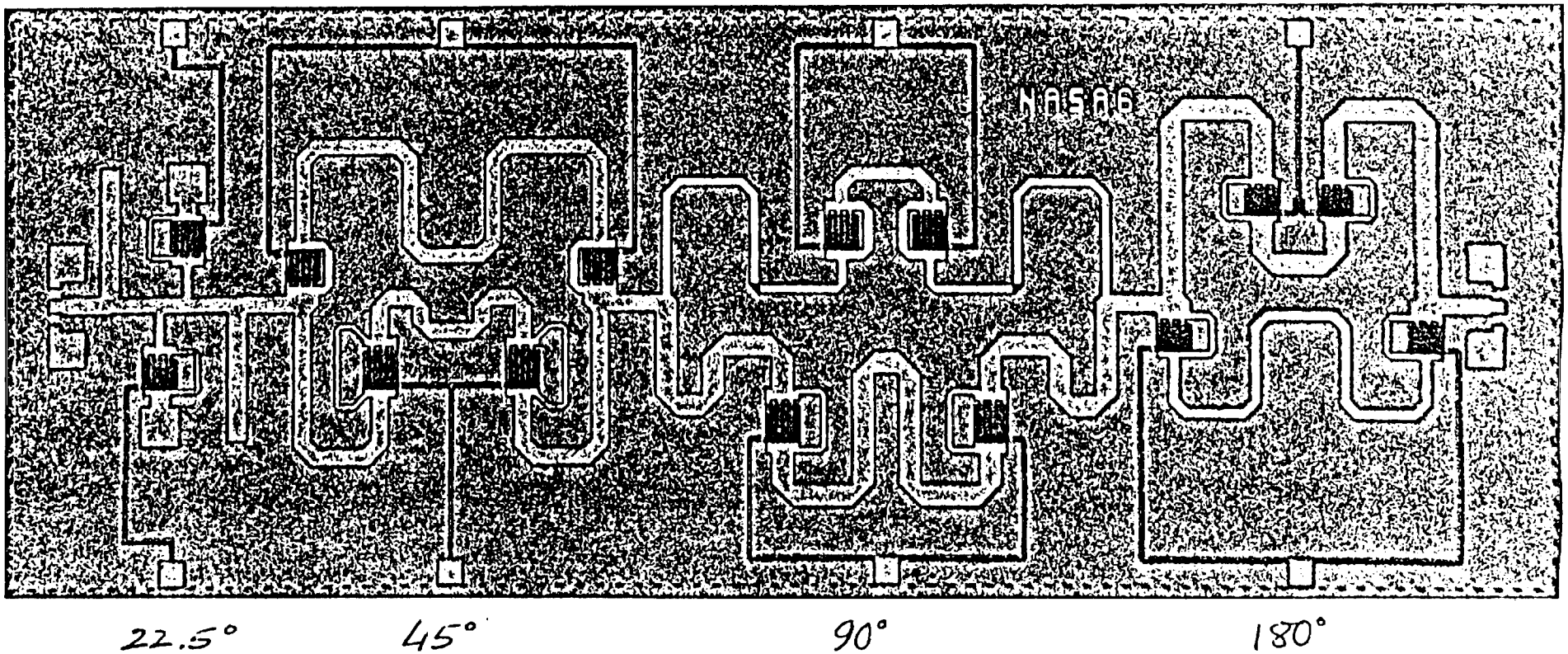


Figure 2-69 4-bit phase shifters; 3-switched line bits and one loaded line bit.

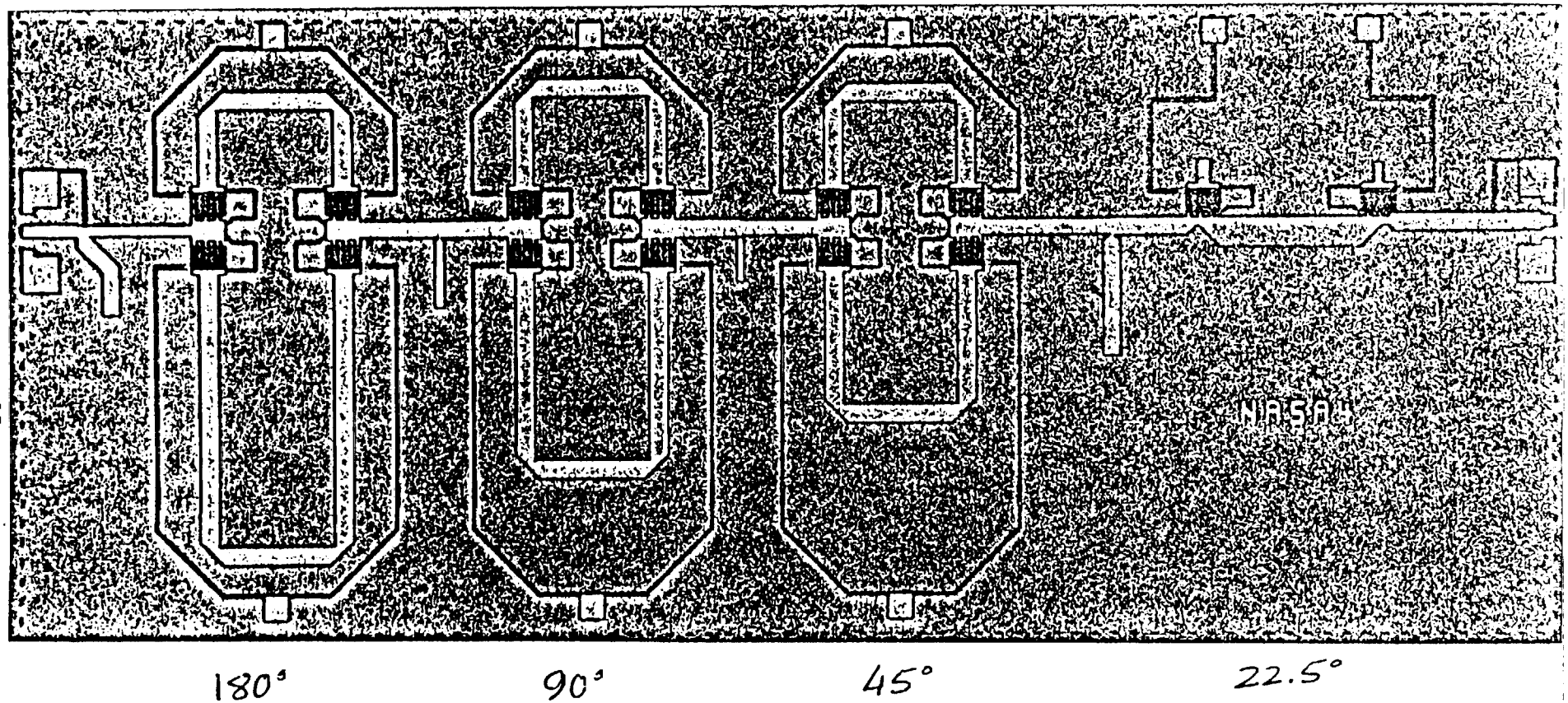


Figure 2-70 4-bit phase shifters; 3 modified switched line bits and one loaded line bit.

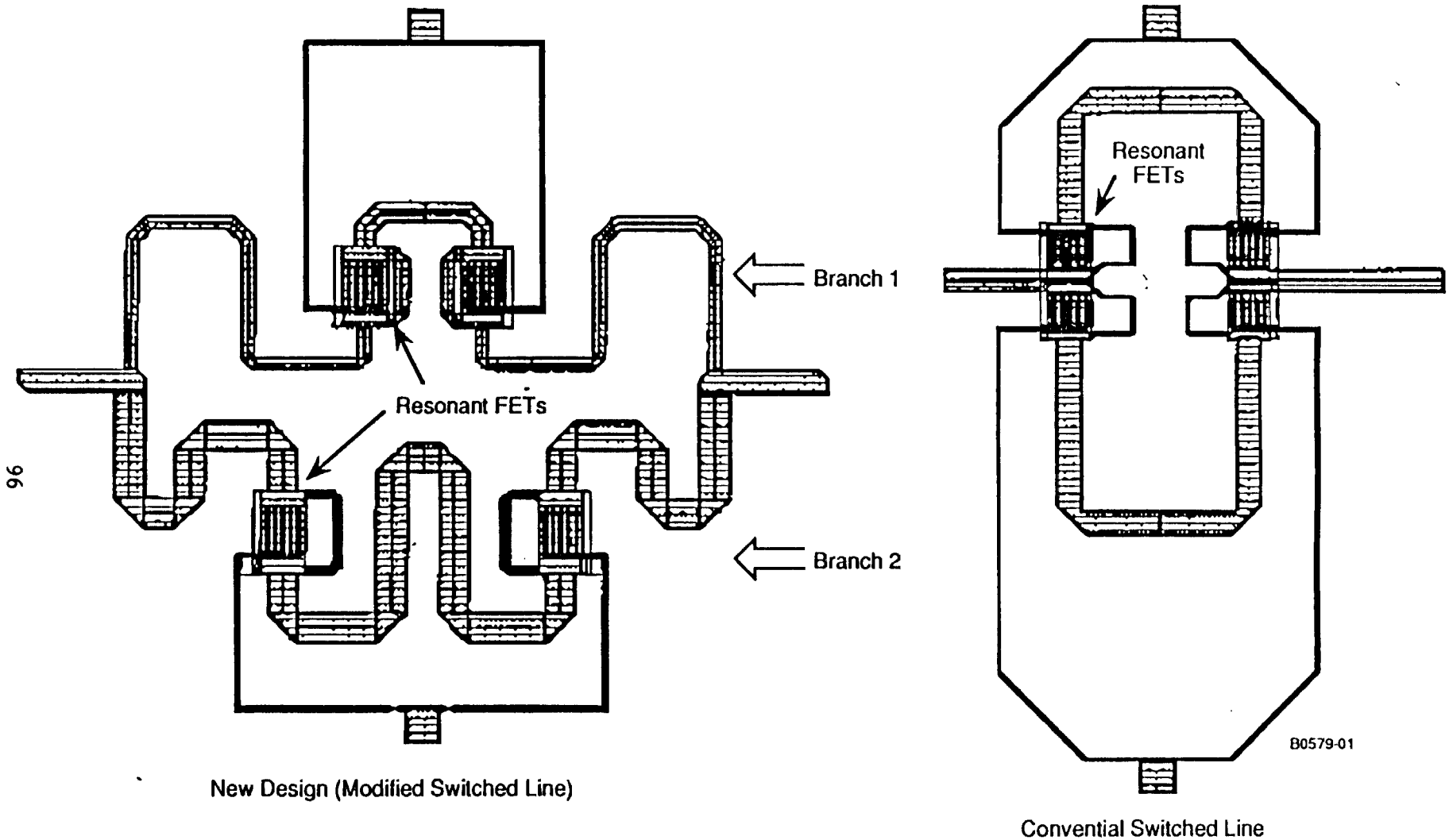
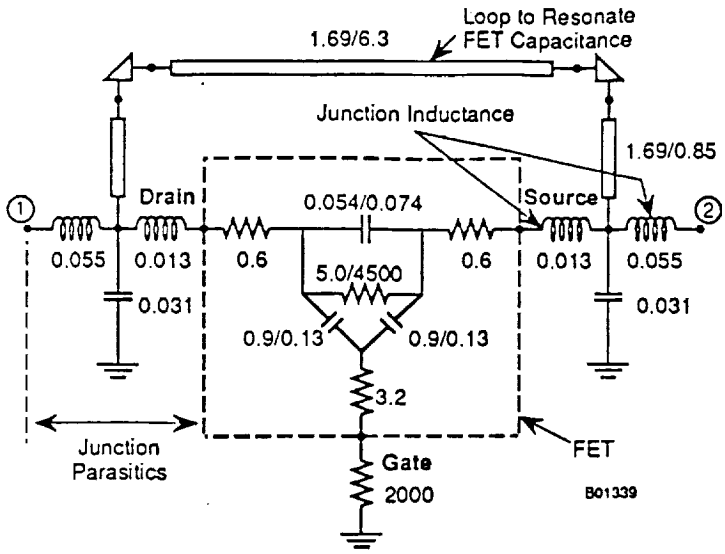


Figure 2-71 Difference in 90° bits between conventional switched line and modified switched line.



Total Gate Periphery is 24 mil (610 μm).
Cap in pf. ind in nh and res in Ohm.
Values for transmission line is width/length in mils.
Values for cap and res are given as ON/OFF states.

ON: VDS = 0 VGS = 0 V
OFF: VDS = 0 VGS = -5 V

Fig. 4 (a). Branch #1 FETs Model

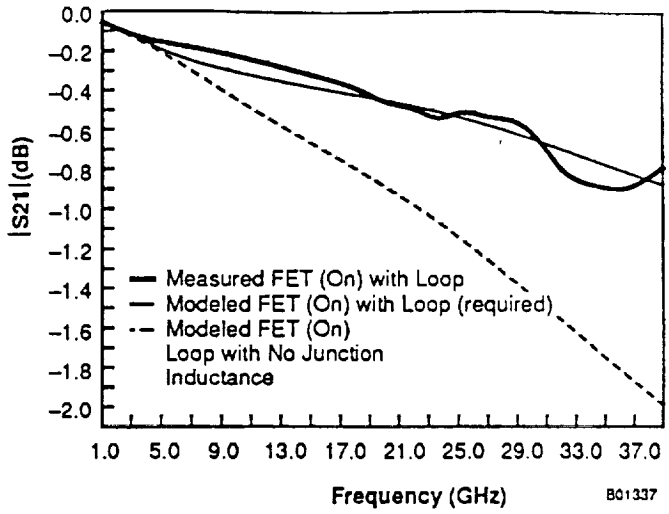


Fig. 4 (b). ON State Modeling of Branch #1 FETs

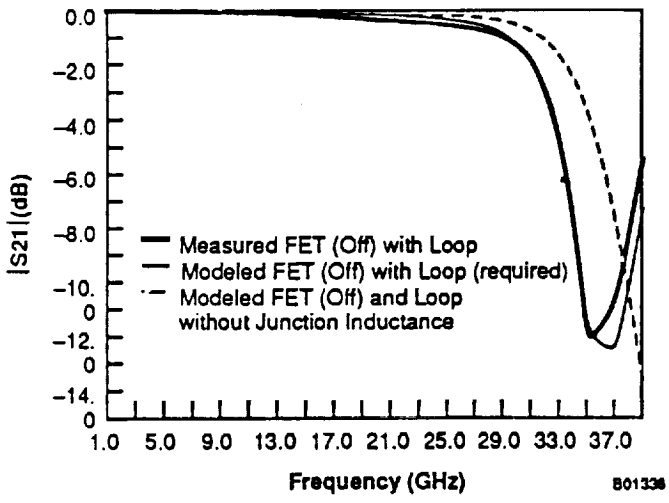


Fig. 4 (c). OFF State Modeling of Branch #1 FETs

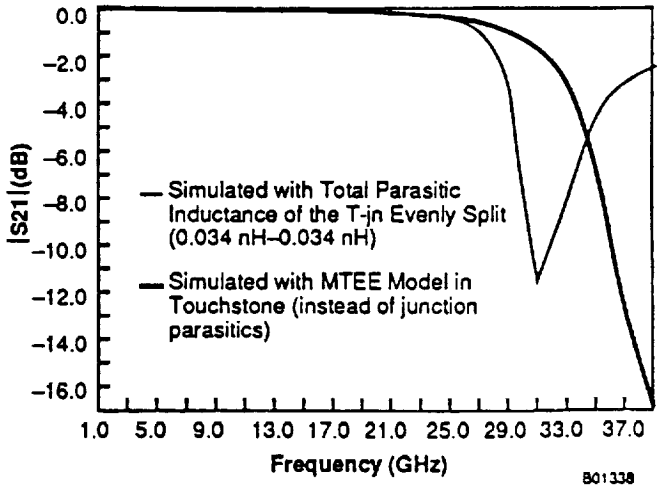
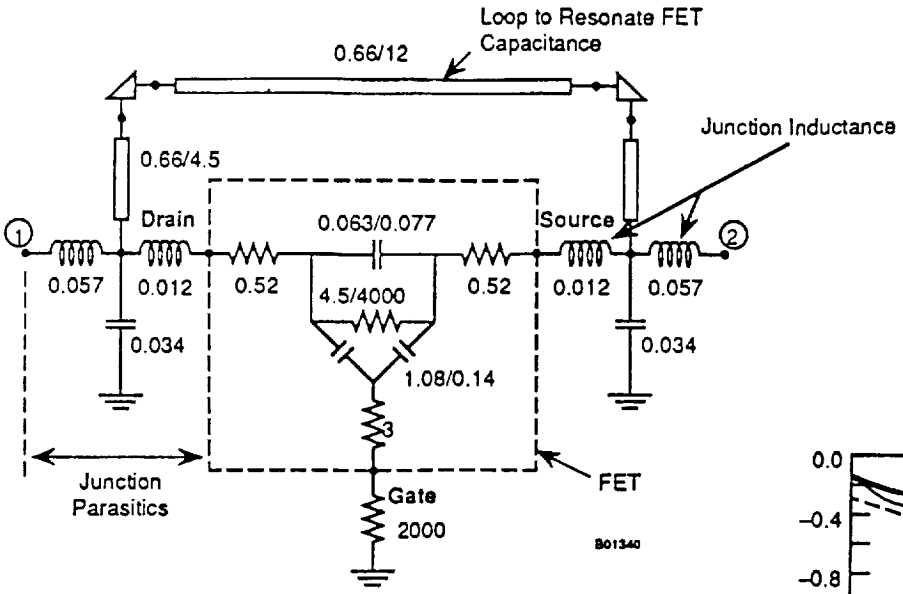


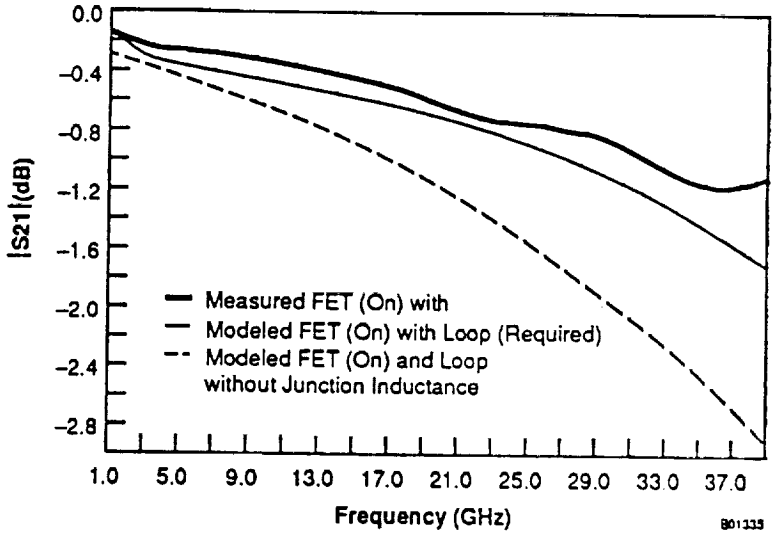
Fig. 4 (d). Modeling Comparison for Branch #1 in "OFF" State

Figure 2-72 a) Branch #1 FET model with loop.
b) ON state modeling of branch #1 FETs.
c) OFF state modeling of branch #2 FETs.
d) Modeling comparison with other two approaches.

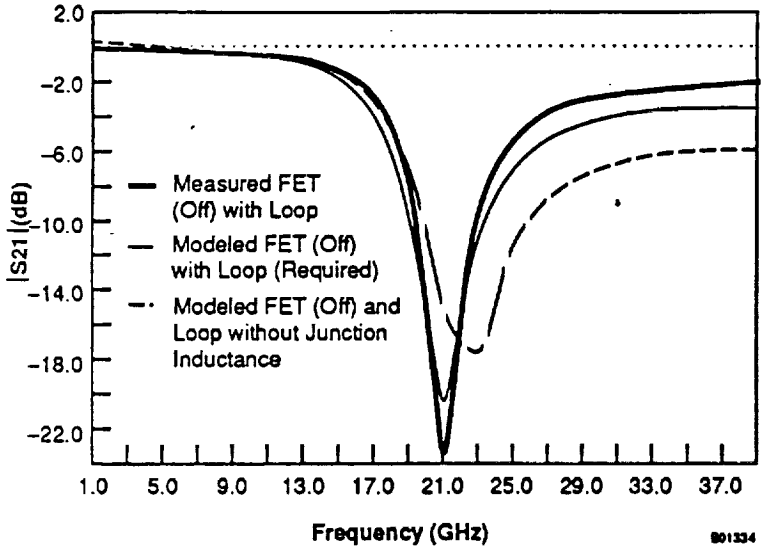


Total FET gate periphery is 26 mil (650 μm).
Other labeling conventions are same as in Fig. 4.

(a)



(b)



(c)

Figure 2-73 a) Branch #2 FET model with loop.
b) ON state modeling of branch #2 FETs.
c) OFF state modeling of branch #2 FETs.

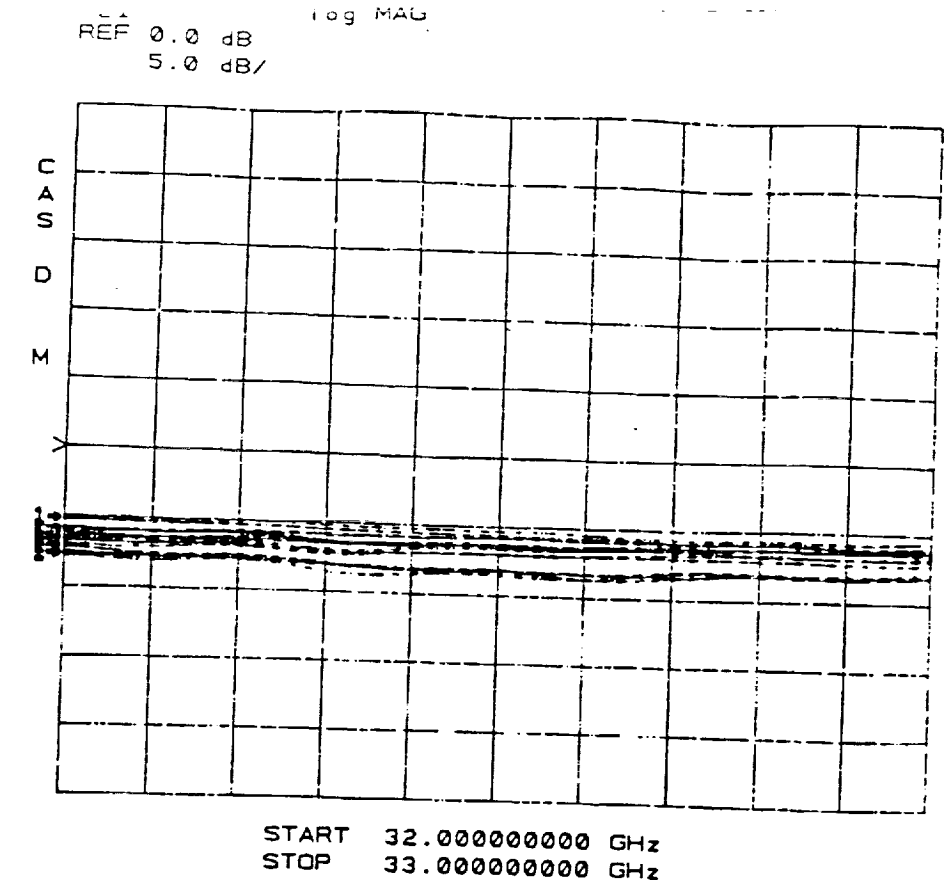


Figure 2-74 a) Measured insertion loss for modified switched line.

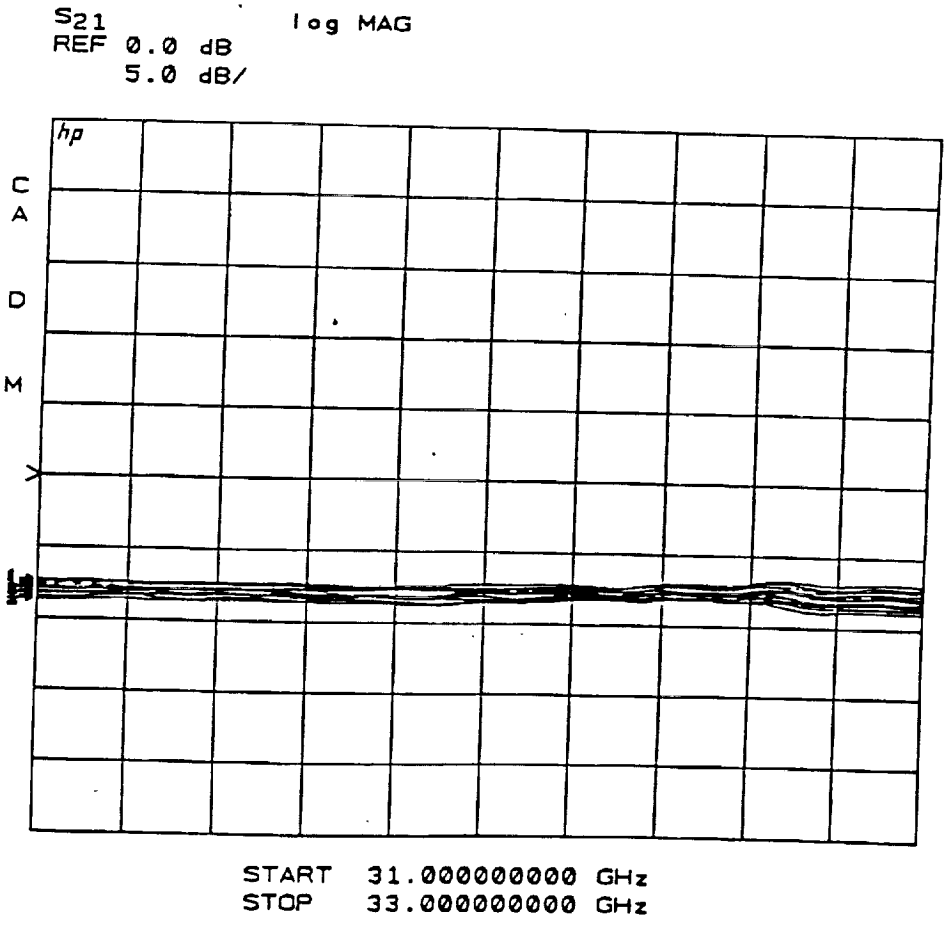


FIGURE 2-74 b) Measured insertion loss for conventional switched line.

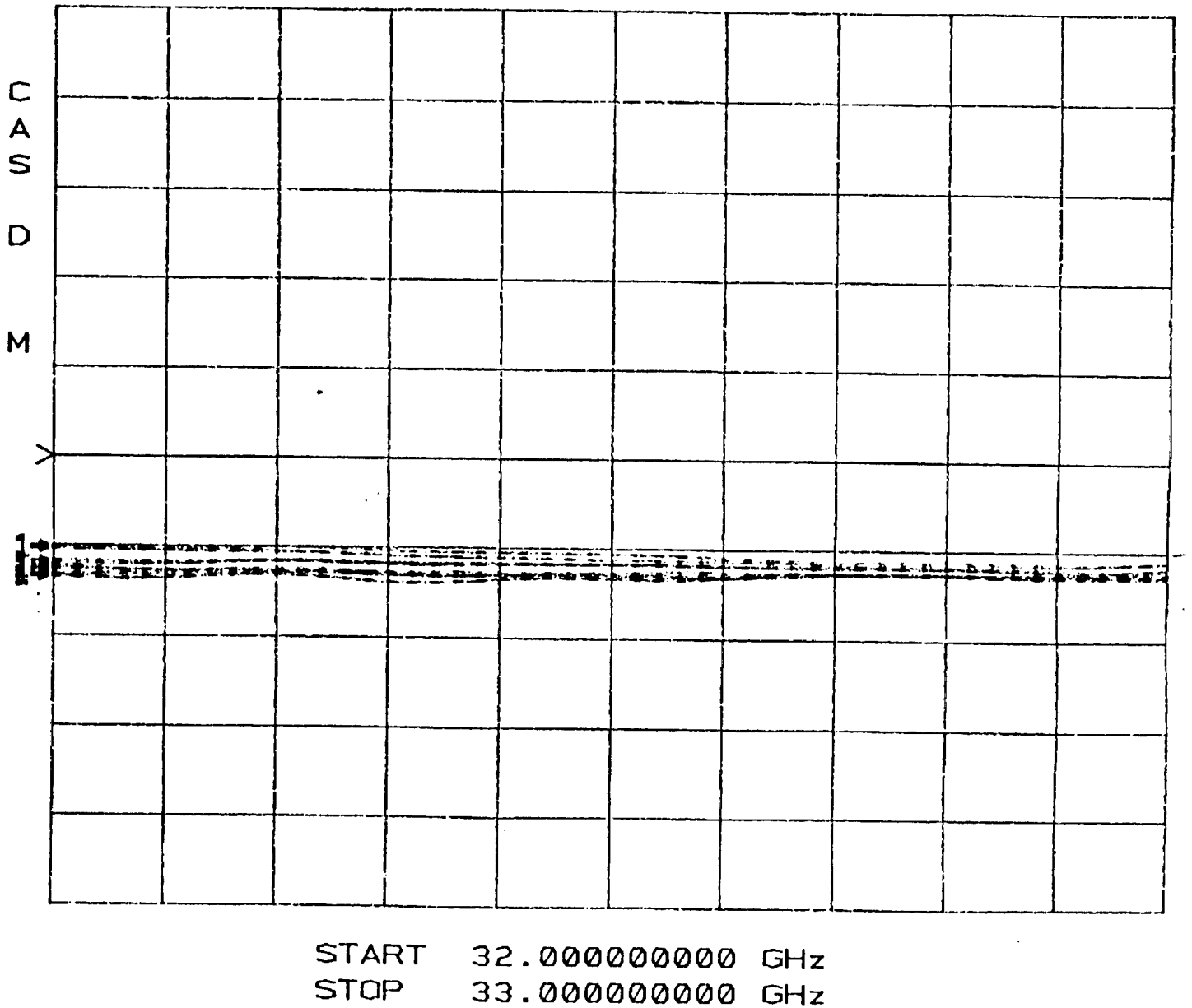


Figure 2-75 Measured insertion loss of modified switched line design with the loaded line bit (22.5°) off

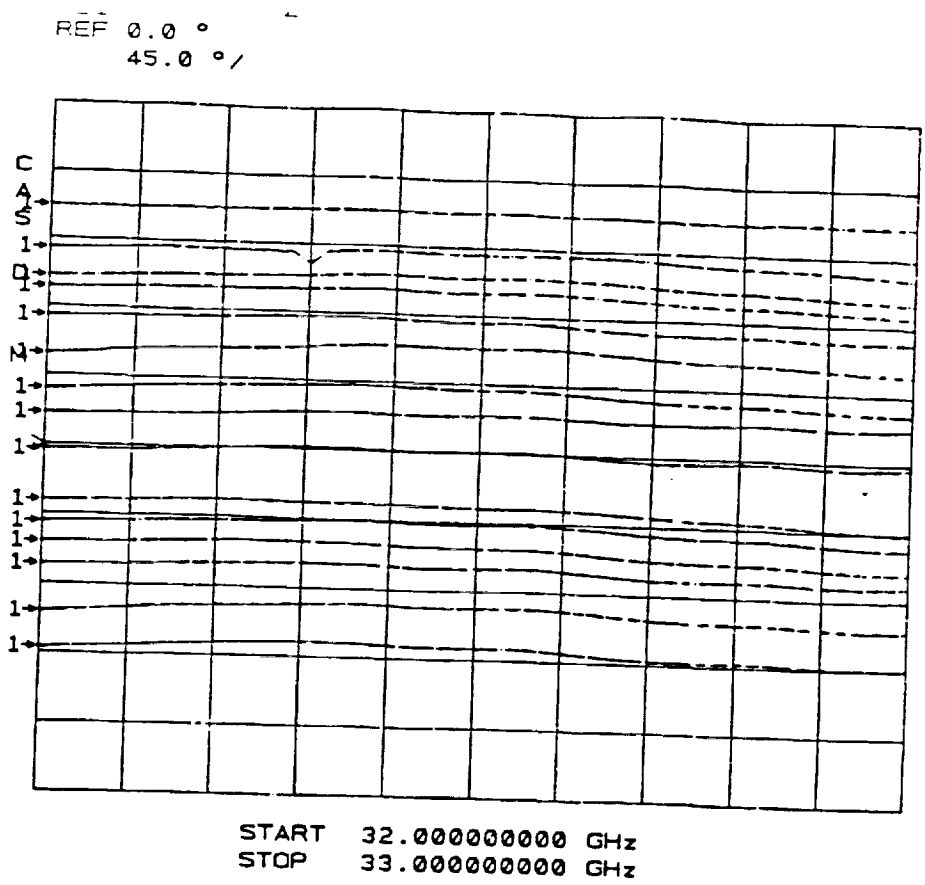


Figure 2-76 a) Phase response of modified switched line model.

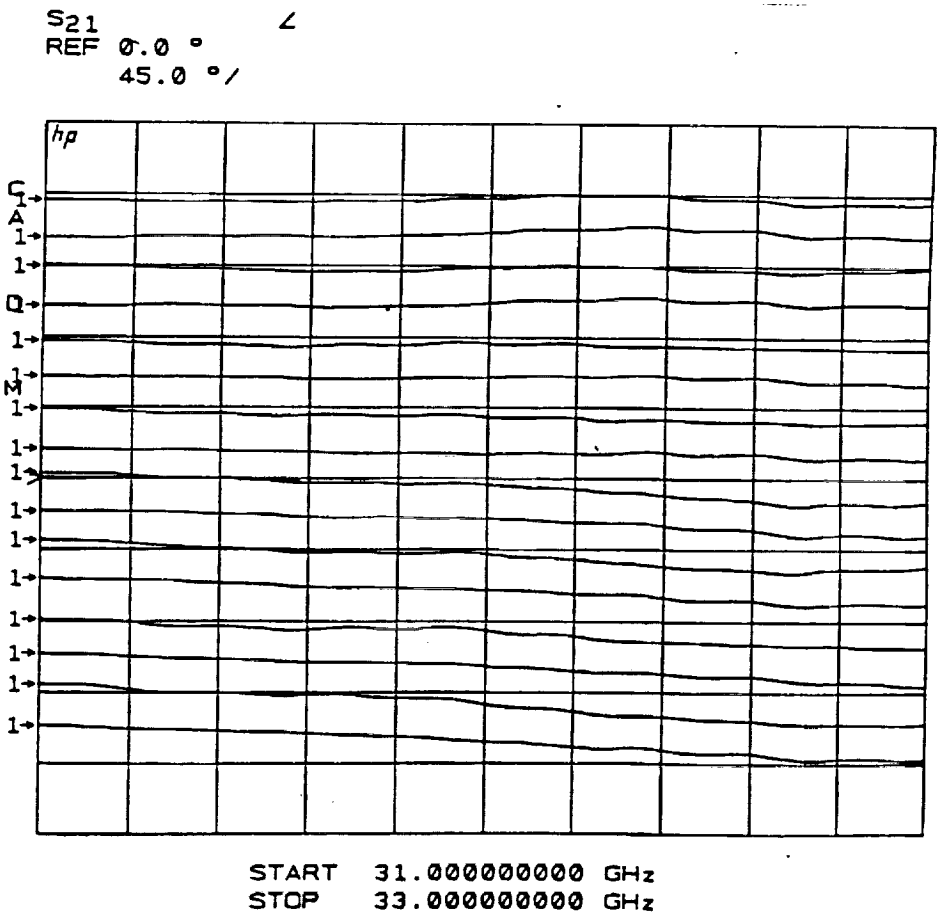


FIGURE 2-76 b) Phase response of conventional switched line model.

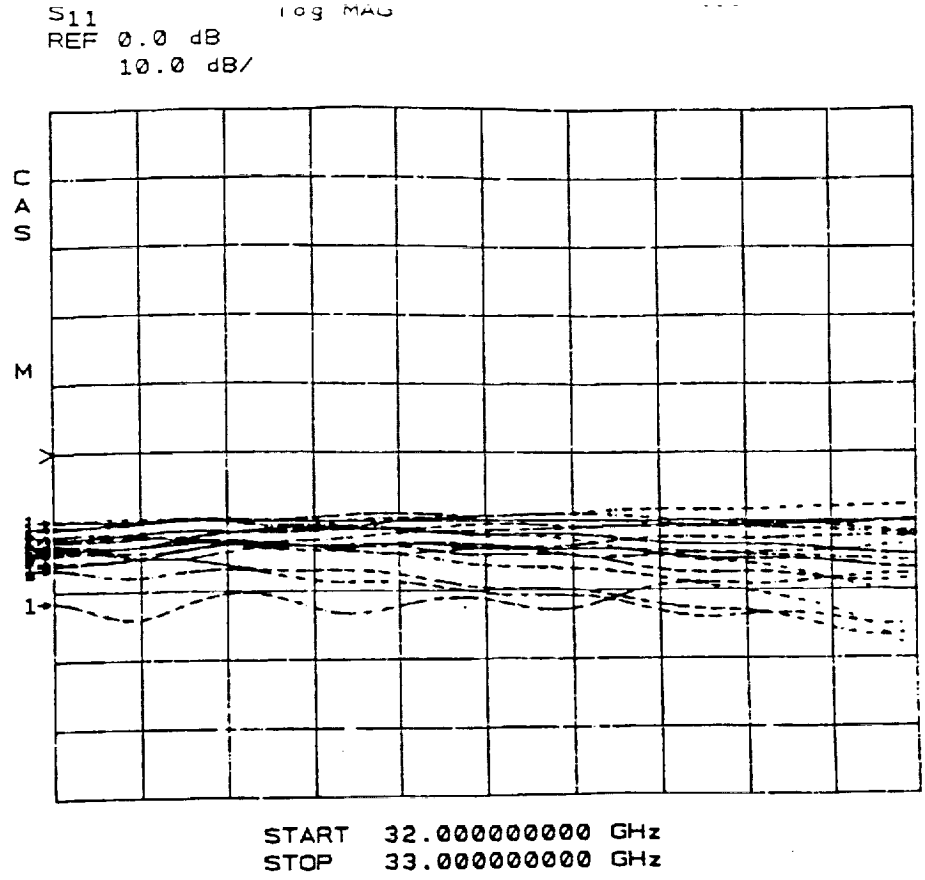


Figure 2-77 a) Reflection at port #1 (180° bit side) for the modified switched line type.

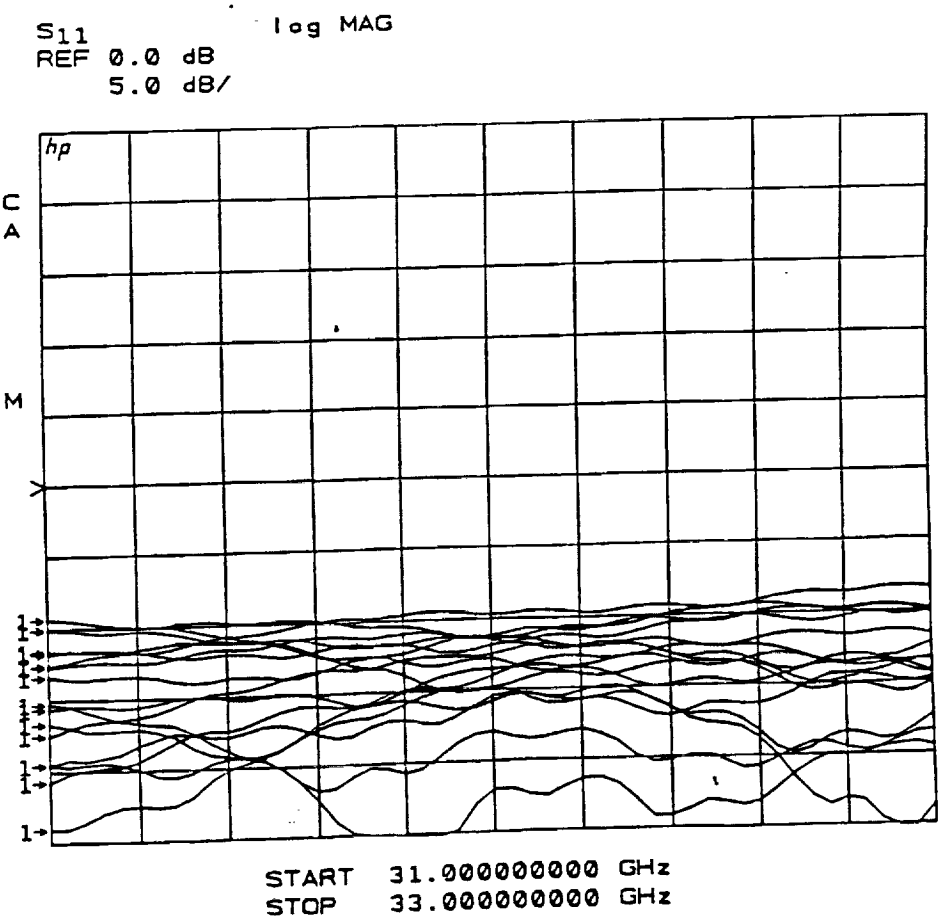


FIGURE 2-77 b) Reflection at port #1 (180° bit side) for the conventional switched line type.